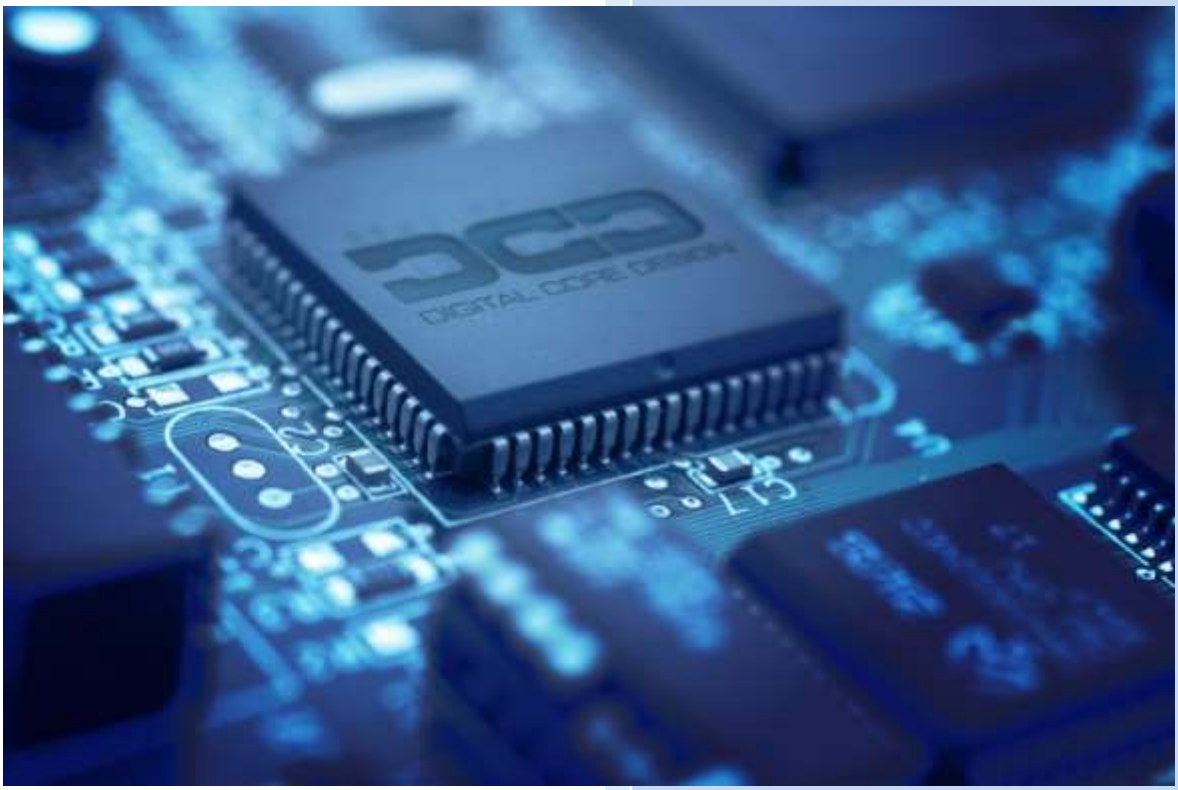
DIGITAL CORE DESIGN

2017

D16752 IP Core



Configurable UART with FIFO v. 1.00

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The D16752 is a universal asynchronous receiver/transmitter (UART), with 64-byte FIFOs and automatic hardware/software flow control. Characters can be programmed to be 5, 6, 7, or 8 bits. The UART has a 64-byte receive FIFO and transmit FIFO and can be programmed to interrupt at different trigger levels. The UART generates its own desired baud rate, based upon a programmable divisor and its input clock. It can transmit even, odd, or no parity and 1, 1.5, or 2 stop bits. The receiver can detect break, idle, or framing errors, FIFO overflow and parity errors. The transmitter can detect a FIFO underflow. The UART also contains a software interface for modem control operations and has a software and hardware flow control capabilities. The D16752 is software compatible with the TL16C752. It provides few enhanced features, which are provided through a special, enhanced feature register. The IP has a selectable hardware and software flow control. The hardware flow control significantly reduces software overhead and increases system efficiency; by automatic control of the serial data flow by using the RTS output and CTS input signals. The software flow control automatically controls the data flow by using programmable Xon/Xoff characters. The UART include a programmable baud rate generator, which can divide the timing reference clock input by a divisor between 1 and (2^{16-1}). **The D16752 can operate as dual channels UART, as well as a single channel UART**.

KEY FEATURES

- Software compatible with 16752 UARTs
- Configuration capability
- Two UART channels - configurable
- Separate configurable BAUD clock line
- Software/Hardware flow control:
- Programmable Xon/Xoff characters
- Programmable AutoRTS, AutoCTS
- Programmable and selectable Transmit and Receive FIFO Trigger levels, for DMA and interrupt generation
- Programmable Receive FIFO Trigger Levels for Software/Hardware Flow Control
- Software Flow Control Turned OFF, optionally by any X on R x Character
- Software Selectable Baud Rate Generator Pre-scalable Clock Rates of 1 x and 4 x
- Programmable SLEEP Mode
- Two modes of operation: UART and FIFO
- Majority Voting Logic
- In the FIFO mode, transmitter and receiver are each buffered with 64 byte FIFO, to reduce the number of interrupts presented to the CPU
- Optional FIFO size extension to 128, 256 or 512 Bytes
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data
- In a UART mode, receiver and transmitter are double buffered, to eliminate the need for precise synchronization between the CPU and serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- False start bit detection
- 16 bit programmable baud generator
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully programmable serial-interface characteristics:
  - *5-, 6-, 7-, or 8-bit characters*
  - *Even, odd, or no-parity bit generation and detection*
  - *1-, 1½-, or 2-stop bit generation*
  - *Baud generation*
- Complete status reporting capabilities
- Line-break generation and detection. Internal diagnostic capabilities:
  - *Loop-back controls for communications link fault isolation*
  - *Break, parity, overrun, framing error simulation*
- Two DMA Modes allows single and multi-transfer
- Technology independent HDL Source Code
- Full prioritized interrupt system controls
- Fully synthesizable static design with no internal tri-state buffers

OPTIONAL FEATURES

- IEEE 1284 Bidirectional Parallel Data Port
  - *Compatible with Standard Centronics Parallel Interface*
  - *Support for Parallel Protocols: ECP and EPP*
  - *Data Path 16/64-Byte FIFO Buffer*
  - *Direct Memory Access (DMA) Transfer*
  - *Decompression of Run Length Encoded Data in ECP Reserve Mode*
  - *Direct Connection to Printer, No External Transceiver is needed*
- Serial Ports with Infrared Data Association (IRDA) inputs and outputs

DESIGN FEATURES

The functionality of the D16752 core was based on the Texas Instruments' TL16C752. The following characteristics differentiate the D16752 from Texas Instruments' devices:

- The bi-directional data bus has been split into two separate buses: datai (7:0), datao (7:0)
- The DLL, DLM and THR registers are reset to all zeros
- TEMT and THRE bits of Line Status Register, are reset during the second clock rising edge following a THR write
- Asynchronous microcontroller interface is replaced by equivalent Universal interface
- All latches implemented in original 16752 devices are replaced by equivalent flip-flop registers, with the same functionality

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF
- VHDL & VERILOG test bench environment
- Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates, minor and major versions changes
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods **without royalty-per-chip fees** make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.

Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core:

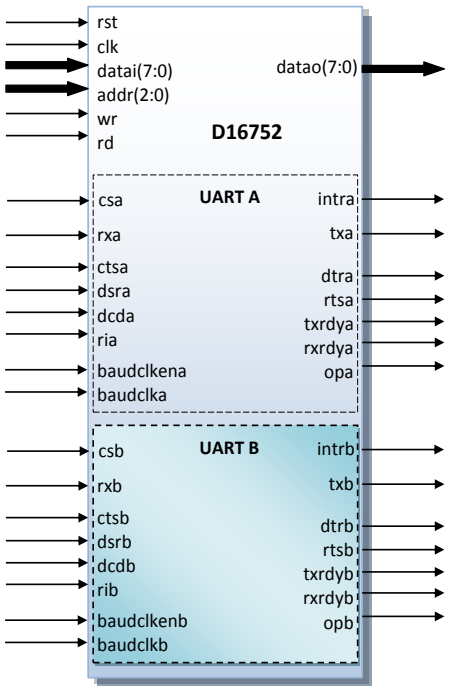
- VHDL or Verilog RTL synthesizable HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM Netlist

CONFIGURATION

The following parameters of the D16752 core can be easily adjusted to requirements of dedicated application and technology. Configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

• Baud generator	- enable - disable
• External RCLK source	- enable - disable
• External BAUDCLK source	- enable - disable
• Modem Control logic	- enable - disable
• SCR Register	- enable - disable
• FIFO Control logic	- enable - disable
• FIFO size	- standard 64 - large up to 512

SYMBOL



PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
rst	input	Global reset
clk	input	Global clock
datai[7:0]	input	Parallel data input
addr[2:0]	input	Address bus
wr	input	Write input
rd	input	Read input
datao[7:0]	output	Parallel data output

UART A pins		
csa	input	Chip select input
rxa	input	Serial data input
ctsa	input	Clear to send input
dsra	input	Data set ready input
dcda	input	Data carrier detect input
ria	input	Ring indicator input
audclkena	input	Baud generator clock enable
baudclka	input	Baud generator clock
intra	output	Interrupt request output
txa	output	Serial data output
dtra	output	Data terminal ready output
rtsa	output	Request to send output
txrdya	output	Transmitter ready output
rxrdya	output	Receiver ready output
opa	output	User Defined Output

UART B pins		
csb	input	Chip select input
rxb	input	Serial data input
ctsb	input	Clear to send input
dsrb	input	Data set ready input
dcdb	input	Data carrier detect input
rib	input	Ring indicator input
baudclkenb	input	Baud generator clock enable
baudclkb	input	Baud generator clock
intrb	output	Interrupt request output
txb	output	Serial data output
dtrb	output	Data terminal ready output
rtsb	output	Request to send output
txrdyb	output	Transmitter ready output
rxrdyb	output	Receiver ready output
opb	output	User Defined Output

UNITS SUMMARY

Data Bus Buffer - The data Bus Buffer accepts inputs from the system bus and generates control signals for other D16752 functional blocks. Address bus ADDR (2:0) selects one of the register to be read from/written into. Both, RD and WE signals, are active low and are qualified by CSA / CSB; RD and WE are ignored, unless the D16752 has been selected by holding CSA/CSB low.

Baud Generator - The D16752 contains a programmable 16 bit baud generator that divides clock input by a divisor in the range, between 1 and (2^{16}–1). The output frequency of the baud generator is 16 × the baud rate. The formula for the divisor is:

$$divisor = \frac{frequency}{baudrate * 16}$$

Two 8-bit registers, called divisor latches DLL and DLM, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the D16752, in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded on the CLK rising edge, following the write to DLL or DLM, to prevent long counts on initial load.

Modem Control Logic controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM).

Interrupt Controller - D16752 contains fully prioritized interrupt system controller. It controls interrupt requests to the CPU and interrupt priority. Interrupt controller contains Interrupt Enable (IER) and Interrupt Identification (IIR) registers.

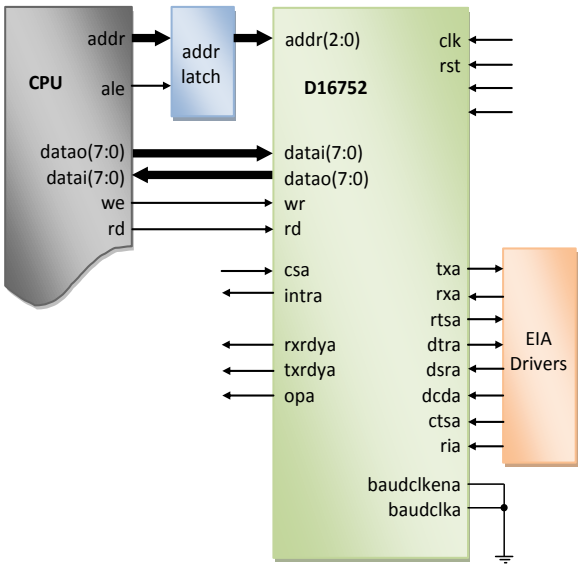
Receiver Control - Receiving starts, when the falling edge on Serial Input (RX) during IDLE State is detected. After starting, the R X input is sampled every 16 internal baud cycles, as it is shown in figure above. When the logic 1 state is detected during START bit, it means that the False Start bit was detected and receiver is back to the IDLE state.

Receiver FIFO - The R x FIFO can be 64 (128, 256, 512) levels deep, it receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time, if R x interrupts are enabled, the UART will issue an interrupt to the CPU. The R x FIFO will continue to store bytes, until it is full and will not accept any more bytes. Any further data entering the R x shift register will set the Overrun Error flag.

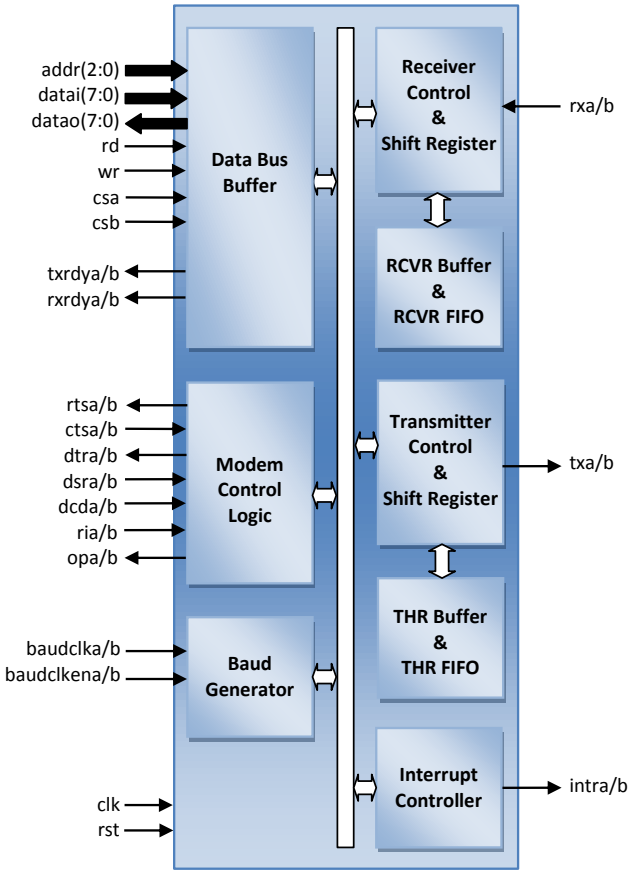
Transmitter Control module controls transmission of written to THR (Transmitter Holding register) character via serial output T X. The new transmission starts on the next overflow signal of internal baud generator, after writing to THR register or Transmitter FIFO. Transmission control contains THR register and transmitter shift register.

Transmitter FIFO - the T x portion of the UART transmits data through T X, as soon as the CPU loads a byte into the T x FIFO. The UART will prevent loads to the Tx FIFO, if it currently holds 64 (128, 256, 512) characters (depending on FCR (5) bit value and selected FIFO size). Loading to the T x FIFO will be enabled again, as soon, as the next character is transferred to the T x shift register. These capabilities account for the largely autonomous operation of the T x. The UART starts the above operations typically with a T x interrupt.

APPLICATION



BLOCK DIAGRAM



DCD'S UART FAMILY OVERVIEW

The family of DCD's UART IP Cores combines high performance, low cost and a small compact size, offering best price/performance ratio in the IP Market. DCD's Cores are designed to be used in cost-sensitive consumer products, such as computer peripherals, office automation, automotive control systems, security and telecommunication applications. Our Cores are written in pure VHDL/VERILOG HDL languages, what makes them technologically independent. All DCD's UART IP Cores can be fully customized according to customer's needs.

Design	SDLC	Synchronous Transmission	FIFO Size (Bytes)	Separate BAUD Clock	Soft Flow Control – Xon/Xoff	RTS/CTS Flow Control	MODEM Control	False START detection	Complete status report	Internal diagnostic	Prioritized interrupts	Break gen. and detect	Half-Duplex RS485	IRDA Port	1284 Parallel Port
DUART	-	-	-	✓	-	-	-	✓	✓	✓	-	-	-	-	-
D2692	-	-	2*8	-	-	✓	-	✓	✓	✓	✓	✓	✓	-	-
D16450	-	-	-	✓	-	-	-	✓	✓	✓	✓	✓	-	-*	-*
D16550	-	-	2* 16	✓	-	-	-	✓	✓	✓	✓	✓	-	-*	-*
D16750	-	-	2* 64	✓	-	✓	✓	✓	✓	✓	✓	✓	*	*	*
D16552	-	-	2* 16	✓	-	-	-	✓	✓	✓	✓	✓	-	✓	✓
D16752	-	-	2* 64	✓	✓	✓	✓	✓	✓	✓	✓	✓	*	*	*
D16950	-	-	2* 128	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	*
D85C30	✓	✓	4	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	-	-

-Optional

PERFORMANCE

The following table gives a survey about the Core area and performance in XILINX® devices after Place & Route:

Device	Speed grade	Slices	F_{max}
VIRTEX-IV	-11	864+4RAMs	125 MHz
VIRTEX-IIP	-7	854+4RAMs	125 MHz
VIRTEX-II	-6	854+4RAMs	100 MHz
VIRTEX-E	-8	856+4RAMs	72 MHz
VIRTEX	-6	856+4RAMs	56 MHz
SPARTAN-IIIE	-5	867+4RAMs	70 MHz
SPARTAN-III	-5	854+4RAMs	83 MHz
SPARTAN-IIE	-7	856+4RAMs	69 MHz
SPARTAN-II	-6	856+4RAMs	69 MHz

[1]- FIFOs implemented in RAM's – 2432 Bits

Core performance in XILINX® devices

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