



2017

DQ8051 IP Core



Revolutionary Quad-Pipelined Ultra High Performance 8-bit Microcontroller v. 6.00

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DQ8051 is an **ultra-high performance, speed optimized** soft core of a single-chip 8-bit embedded controller, designed to operate with fast (typically on-chip) and slow (off-chip) memories. The core has been designed with a special concern about performance to power consumption ratio. This ratio is extended by an **Advanced Power Management Unit** – the **PMU**. The DQ8051 soft core is 100% binary-compatible with the 8051 industry standard 8-bit microcontroller. The DQ8051 has a built-in configurable **DoCD - JTAG on-chip debugger**, supporting **Keil µVision development** platform and a standalone DoCD debug software. **Dhrystone 2.1 benchmark program runs from 19.69 to 26.62 times faster than the original 80C51 at the same frequency.** This performance can also be exploited to a great advantage in low power applications, where the core can be clocked over ten times more slowly than the original implementation, with no performance penalty. The DQ8051 is fully customizable - it is delivered in the exact configuration, to meet your requirements. The DQ8051 is delivered with **fully automated test bench** and **complete set of tests**, allowing easy package validation at each stage of SoC design flow.

CPU FEATURES

- 100% software compatible with the 8051 industry standard
- Quad-Pipelined architecture enables to execute 26.62 times faster than the original 80C51 at the same frequency
- Up to 25.053 VAX MIPS at 100 MHz
- 24 times faster multiplication
- 12 times faster addition
- 2 Data Pointers (DPTR) for faster memory blocks copying
 - *Advanced INC & DEC modes*
 - *Auto-switch of current DPTR*
- Up to 256 bytes of internal (on-chip) Data Memory - IDM
- Up to 64K bytes of Program Memory
- Up to 16M bytes of external (off-chip) Data Memory - XDM
 - *Synchronous interface for up to 64K bytes of (on-chip) fast external Data Memory - (SXDM)*
- User programmable Program Memory Wait States solution for wide range of memories speed
- User programmable External Data Memory Wait States solution for wide range of memories speed
- De-multiplexed Address/Data bus to allow easy connection to memory

- Interface for additional Special Function Registers
- Fully synthesizable, static synchronous design with no internal tri-states
- Scan test ready

PERIPHERALS

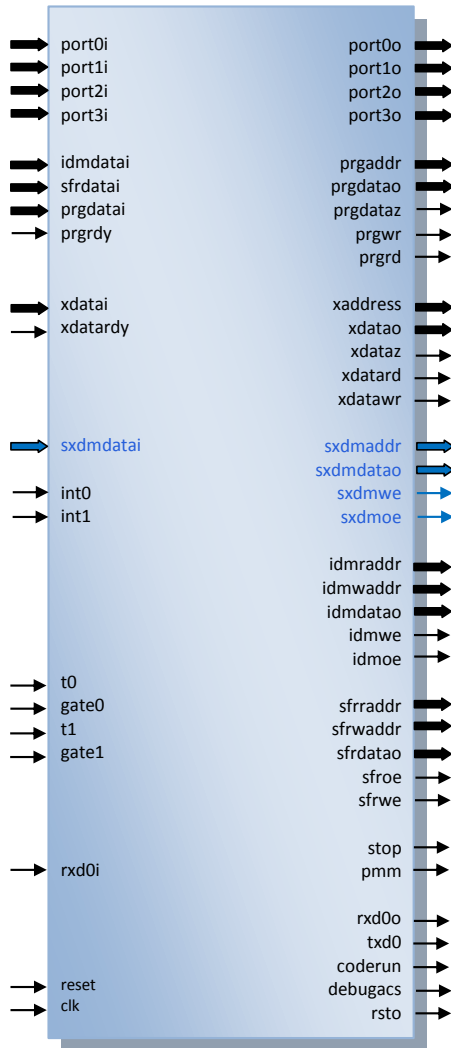
- DoCD™ debug unit
 - *Processor execution control*
 - *Run, Halt*
 - *Step into instruction*
 - *Skip instruction*
 - *Read-write all processor contents*
 - *Program Counter (PC)*
 - *Program Memory*
 - *Internal (direct) Data Memory*
 - *Special Function Registers (SFRs)*
 - *External Data Memory*
 - *Code execution breakpoints*
 - *up to eight real-time PC breakpoints*
 - *unlimited number of real-time OP CODE breakpoints*
 - *Hardware execution watch-points at*
 - *Internal (direct) Data Memory*
 - *Special Function Registers (SFRs)*
 - *External Data Memory*
 - *Hardware watch-points activated at certain*
 - *address by any write into memory*
 - *address by any read from memory*
 - *address by write into memory a required data*
 - *address by read from memory a required data*
 - *Instructions Smart Trace Buffer – configurable up to 8192 levels (optional)*
 - *Automatic adjustment of debug data transfer speed rate between HAD and Silicon*
 - *JTAG Communication interface*
- Power Management Unit
 - *Power management mode*
 - *Switchback feature*
 - *Stop mode*
- Extended Interrupt Controller
 - *2 priority levels*
 - *2 external interrupt sources*
 - *3 interrupt sources from peripherals*
- Four 8-bit I/O Ports
 - *Bit addressable data direction for each line*
 - *Read/write of single line and 8-bit group*
- Two 16-bit timer/counters
 - *Timers clocked by internal source*
 - *Auto reload 8-bit timers*
 - *Externally gated event counters*
- Full-duplex serial port
 - *Synchronous mode, fixed baud rate*
 - *8-bit asynchronous mode, fixed baud rate*
 - *9-bit asynchronous mode, fixed baud rate*
 - *9-bit asynchronous mode, variable baud rate*

DELIVERABLES

- ◆ Source code:
 - VHDL Source Code or/and
 - VERILOG Source Code or/and
 - Encrypted, or plain text EDIF
- ◆ VHDL & VERILOG test bench environment
 - Active-HDL automatic simulation macros
 - ModelSim automatic simulation macros
 - Tests with reference responses
- ◆ Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
- ◆ Synthesis scripts

- ◆ Example application
- ◆ Technical support
 - IP Core implementation support
 - 3 months maintenance
 - Delivery of the IP Core and documentation updates, minor and major versions changes
 - Phone & email support

SYMBOL



CONFIGURATION

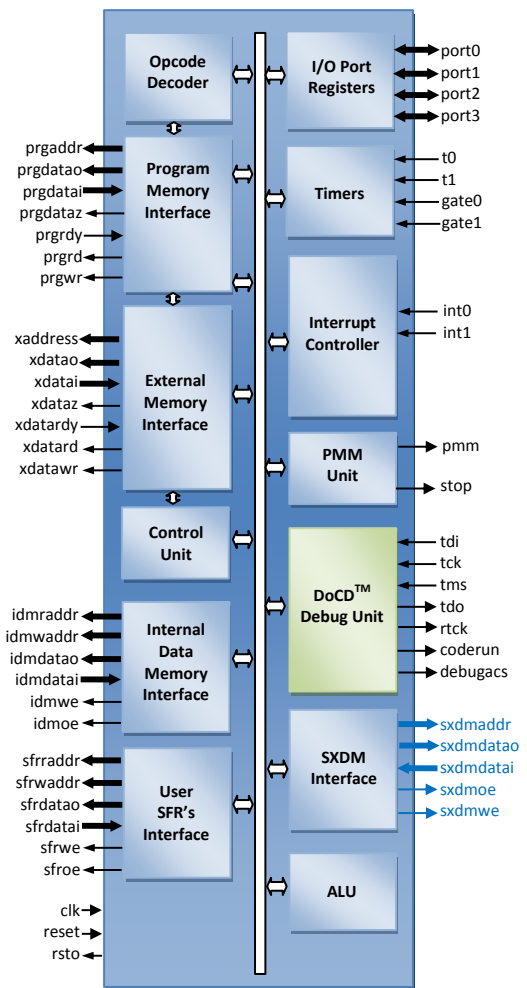
The following parameters of the DQ8051 core can be easily adjusted to requirements of a dedicated application and technology. The configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

- Second Data Pointer (DPTR1)
 - used
 - unused
- DPTR0 decrement
 - used
 - unused
- DPTR1 decrement
 - used
 - unused
- Data Pointers auto-switch
 - used
 - unused
- Data Pointers auto-update
 - used
 - unused
- **Interrupts**
 - subroutines location

- Power Management Mode
 - used
 - unused
- Stop mode
 - used
 - unused
- Peripherals
 - used
 - unused
- Synchronous XDM
 - size
- DoCD™ debug unit
 - used
 - unused

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate constants in the package file.

BLOCK DIAGRAM



DESIGN FEATURES

- ◆ **PROGRAM MEMORY:**
The DQ8051 soft core is dedicated for operation with Internal or External Program Memory. Program Memory can be implemented as ROM, RAM or FLASH.
- ◆ **INTERNAL DATA MEMORY:**
The DQ8051 can address Internal Data Memory of up to 256 bytes. The Internal Data Memory can be implemented as synchronous RAM.
- ◆ **EXTERNAL DATA MEMORY:**
The DQ8051 soft core can address up to 16 MB of External Data Memory. Extra DPX (*Data Pointer eXtended*) register is used for segments swapping.

◆ SYNCHRONOUS XDM:

The DQ8051 soft core can address up to 64 kB of fast on-chip Synchronous External Data Memory. All reads and writes are executed in one clock cycle.

◆ USER SPECIAL FUNCTION REGISTERS:

Up to 60 External (user) Special Function Registers (ESFRs) may be added to the DQ8051 design. ESFRs are memory mapped into Direct Memory between addresses 0x80 and 0xFF, in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR.

◆ WAIT STATES SUPPORT:

The DQ8051 soft core is dedicated to operate with wide range of Program and Data memories. Slow Program and External Data memory may assert a memory Wait signal to hold up CPU activity.

UNITS SUMMARY

ALU – Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic, like arithmetic unit, logic unit, multiplier and divider.

Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks.

Control Unit – It performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and it manages the execution of all microcontroller tasks.

Program Memory Interface – Contains Program Counter (PC) and related logic. It performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader, to load new program into ROM, RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C or DoCD™ module.

External Data Memory Interface - Contains memory access related registers, such as Data Pointer High (DPH), Data Pointer Low (DPL), Data Page Pointer (DPP), MOVX @Ri address register (MXAX) and STRETCH registers. It performs the memory addressing and data transfers. It also allows applications software to access up to 16 MB of external data memory. The DPP register is used for segments swapping. STRETCH register allows flexible timing management, while accessing different speed system devices, by programming XDATAWR and XDATARD pulse width between 1 and 8 clock periods.

Synchronous eXternal Data Memory (SXDM) Interface – contains XDATA memory access related logic, allowing fast access to synchronous memory devices. It performs the external Data Memory addressing and data transfers. This memory can be used to store large variables, frequently accessed by CPU, improving overall performance of application.

Internal Data Memory Interface – Controls an access to the internal memory of size up to 256 bytes. It contains 8-bit Stack Pointer (SP) register and related logic.

User SFRs Interface – Special Function Registers interface controls access to the special registers. It contains standard and user defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified), by using all direct addressing mode instructions.

Interrupt Controller – Responsible for the interrupt management system of external and internal interrupt sources. It contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IP) and (TCON) registers.

I/O Ports – The block contains 8051's general purpose I/O ports. Each of port's pin can be read/write as a single bit or as an 8-bit bus called P0, P1, P2, and P3.

Power Management Unit – Contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. Switchback feature allows UARTs and interrupts to be processed in full speed mode, if enabled. It's highly desirable, when microcontroller is planned to be used in portable and power critical applications.

DoCD™ Debug Unit – it's a **real-time hardware debugger**, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** ensures **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware watchpoints can be set and controlled on internal and external data memories and also on SFRs. Hardware watchpoints are executed, if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins: CODERUN and DE-BUGACS, indicate the state of the debugger and CPU. CODERUN is active, when CPU is executing an instruction. DE-BUGACS pin is active, when any access is performed by **DoCD™** debugger. The **DoCD™** system includes **JTAG interface** and complete set of tools, to communicate and work with core in real time debugging. It is built, as a scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off.

Timers – System timers module. Contains two 16bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 (or 4) CLK periods, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.

UART0 – Universal Asynchronous Receiver and Transmitter module is full duplex, which means, that it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning, it can commence reception of the second byte, before the previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register and reading SBUF0, reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART0 can be synchronized by Timer 1 or Timer 2 (if present in system).

DQ8051 FAMILY OVERVIEW

The main features of each DQ8051 family member have been summarized in the table below. It gives a brief member characteristic, helping you to select the most suitable IP Core for your application. You can specify your own peripheral set (including listed below and others) and requests the core modifications.

| Design | Architecture speed grade | Program Memory space | | | Stack space size | Internal Data Memory space | External Data Memory space | External Data / Program Memory Wait States | Power Management Unit | Interface for additional SFRs | Interrupt sources | Interrupt levels | Data Pointers | Timer/Counters | UART | I/O Ports | Compare/Capture | Watchdog | Master I ² C Bus Controller | Slave I ² C Bus Controller | SPI | Fixed Point Coprocessor | Floating Point Coprocessor |
|-----------|--------------------------|----------------------|-------------|----------|------------------|----------------------------|----------------------------|--|-----------------------|-------------------------------|-------------------|------------------|---------------|----------------|------|-----------|-----------------|----------|--|---------------------------------------|-----|-------------------------|----------------------------|
| | | on-chip RAM | on-chip ROM | off-chip | | | | | | | | | | | | | | | | | | | |
| DQ8051CPU | 25.1 | 64k | 64k | 64k | 256 | 256 | 16M | ✓ | ✓ | ✓ | 2 | 2 | 2 | - | - | - | - | - | - | - | - | - | |
| DQ8051 | 25.1 | 64k | 64k | 64k | 256 | 256 | 16M | ✓ | ✓ | ✓ | 5 | 2 | 2 | 2 | 1 | 4 | - | - | - | - | - | - | |
| DQ8051XP | 26.6 | 64k | 64k | 64k | 256 | 256 | 16M | ✓ | ✓ | ✓ | 15 | 2 | 2 | 3 | 2 | 4 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | |

DQ8051 family of Pipelined High Performance Microcontroller Cores

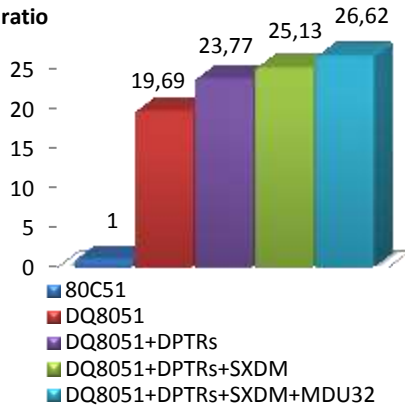
PERFORMANCE

One of the most important performance parameter is a real application speed improvement, comparing to the well-known 80C51 architecture. The Dhrystone Benchmark Version 2.1 was used to measure the 80C51 and the DQ8051 core performance. The following table gives a survey about the DQ8051 performance in terms of Dhrystone VAX MIPS per 1 MHz and its improvement comparing to the 80C51.

| Device | DMIPS/MHz | Ratio |
|-------------------------|-----------|-------|
| 80C51 | 0,00941 | 1,00 |
| DQ8051 | 0,18527 | 19,69 |
| DQ8051+DPTRs | 0,22369 | 23,77 |
| DQ8051+DPTRs+SXDM | 0,23650 | 25,13 |
| DQ8051+DPTRs+SXDM+MDU32 | 0,25053 | 26,62 |

Core performance in terms of DMIPS per MHz

VAX MIPS ratio



The following table gives a survey about the DQ8051 core area in ASIC Devices (CPU features and peripherals included):

| Device | Speed | Min area | F _{max} |
|---------|---------|-------------|------------------|
| 0,35 um | typical | 10500 gates | 70 MHz |
| 0,25 um | typical | 11000 gates | 125 MHz |
| 0,18 um | typical | 10500 gates | 180 MHz |
| 0,13 um | typical | 10700 gates | 260 MHz |
| 0,09 um | typical | 9900 gates | 430 MHz |

DQ8051 core area and performance in ASIC devices.

Results given for working system with two DPTRs and connected 256B IDM, 8kB CODE and 2kB SXDM memories.

Area utilized by the each unit of DQ8051 core in vendor specific technologies is summarized in the table below.

| Component | Area [Gates] |
|------------------------------------|--------------|
| CPU* | 7250 |
| DPTR1 register | 400 |
| DPTR0 decrement | 50 |
| DPTR1 decrement | 50 |
| DPTR's auto-switch and auto-update | 150 |
| SXDM | 75 |
| Interrupt Controller | 150 |
| Power Management Unit | 75 |
| I/O ports | 200 |
| Timers | 700 |
| UART0 | 800 |
| Total area | 9900 |

Core components area utilization

*CPU – consisted of ALU, Opcode Decoder, Control Unit, User SFRs interface, IDM interface, XDM interface and Code Memory interface.

LICENSING

Comprehensible and clearly defined licensing methods **without royalty-per-chip fees** make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.

Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core:

- VHDL or Verilog RTL synthesizable HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM Netlist

CONTACT

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