DSPI IP Core

Serial Peripheral Interface – Master/Slave v. 2.09
COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DSPI is a fully configurable SPI master/slave device, which allows user to configure polarity and phase of a serial clock signal (SCK). It allows the microcontroller to communicate with serial peripheral devices and is also capable of interprocessor communications in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on two independent serial data lines. DSPI data is simultaneously transmitted and received. What’s most important, it’s a technology independent design, which can be implemented in a variety of process technologies. The DSPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. It can be configured as a master or a slave device, with data rates as high as CLK/4. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols, to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, the software selects one of eight different bit rates for the serial clock. The DSPI automatically drives selected by SSCR (Slave Select Control Register) slave outputs (SS70 – SS00) and address SPI slave device, to exchange serially shifted data. Error-detection logic is included, to support interprocessor communications. A write collision detector indicates when an attempt is made to write data to the serial shift register, while transfer is in progress. A multiple-master mode-fault detector automatically disables DSPI output drivers, if more than one SPI devices simultaneously attempts to become a bus master. The DSPI is fully customizable and can be tailored to your configuration and requirements. It includes fully automated testbench with complete set of tests, allowing easy package validation at each stage of SoC design flow.

KEY FEATURES

- SPI Master
  - Master and Multi-master operations
  - 8 SPI slave select lines
  - System error detection
  - Mode fault error
  - Write collision error
  - Interrupt generation
  - Supports speeds up to ¾ of system clock

- SPI Slave
  - Slave operation
  - System error detection
  - Interrupt generation
  - Supports speeds up ¼ of system clock

- Complex interface allows easy connection to microcontrollers

- Fully synthesizable, static synchronous design, with no internal tri-states

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF

- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses

- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet

- Synthesis scripts
- Example application
- Technical support
- IP Core implementation support
- 3 months maintenance
- Delivery of the IP Core and documentation updates, minor and major versions changes
- Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.

Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core:

- VHDL or Verilog RTL synthesizable HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM Netlist

UNITS SUMMARY

Shift register and Read Data Buffer – Central element in the SPI system. The system is single buffered in the transmit direction and double buffered in the receive direction. This fact means that the new data for transmission cannot be written to the shifter, until the previous transaction is complete; however, received data is transferred into a parallel read data buffer, so the shifter is free to accept a second serial character. As long as the first character is read out of the read data
buffer before the next serial character is ready to be transferred, no overrun condition will occur. When an SPI transfer occurs, an 8-bit character is shifted out on data pin, while a different 8-bit character is simultaneously shifted in on a second data pin. Another way to view this transfer is that an 8-bit shift register in the master and another 8-bit shift register in the slave is connected as a circular 16-bit shift register. When the transfer occurs, this distributed shift register is shifted eight bit positions; thus, the characters in the master and slave are effectively exchanged.

**Control Register** may be read or written at any time, it is used to configure the DSPI System. This register controls the mode of transmission (Master, Slave), polarity and phase of SPI Clock and transmission speed.

**Status Register** (SPSR) contains flags, indicating the completion of transfer or occurrence of system errors. All flags are set automatically when the corresponding event occurs and cleared by software sequence.

**Slave Select Control Register** configures which slave select output should be driven while SPI master transfer. Contents of SSCR register is automatically assigned on SS7O-SS00 pins when DSPI master transmission starts.

**SPI Clock Logic** - Software can select any from four combinations of serial clock (SCK) phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers, to allow master device communication with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPI allows direct interface to almost any existing synchronous serial peripheral.

**TRANSFER FORMATS**

The software can select any of four combinations of serial clock (SCK) phase and polarity, using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit, selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers, to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPI allows direct interface to almost any existing synchronous serial peripheral.
**TYPICAL uC / BUS CONNECTION**

The figure below shows a typical connection the DSPI Core with microcontroller and other SPI Master/Slave devices.

![Typical Connection Diagram]

**PERFORMANCE**

The following table gives a survey about the Core performance in INTEL FPGA® devices after Place & Route (all key features included):

<table>
<thead>
<tr>
<th>Device</th>
<th>Speed grade</th>
<th>Logic Cells</th>
<th>Memory Bits</th>
<th>F_{max}</th>
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<tbody>
<tr>
<td>ARIA GX</td>
<td>-6</td>
<td>147/98</td>
<td>-</td>
<td>290 MHz</td>
</tr>
<tr>
<td>ARIA V</td>
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<td>144/115</td>
<td>-</td>
<td>368 MHz</td>
</tr>
<tr>
<td>CYCLONE</td>
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<td>187</td>
<td>-</td>
<td>281 MHz</td>
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<tr>
<td>CYCLONE2</td>
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<td>321 MHz</td>
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<tr>
<td>CYCLONE3</td>
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<td>-</td>
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</tr>
<tr>
<td>CYCLONE4</td>
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<td>170/98</td>
<td>-</td>
<td>250 MHz</td>
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<tr>
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<td>-</td>
<td>327 MHz</td>
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<tr>
<td>STRATIX</td>
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<td>-</td>
<td>306 MHz</td>
</tr>
<tr>
<td>STRATIX2</td>
<td>-3</td>
<td>150/100</td>
<td>-</td>
<td>408 MHz</td>
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<td>-</td>
<td>649 MHz</td>
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<tr>
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<td>144/114</td>
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<tr>
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<td>144/114</td>
<td>-</td>
<td>297 MHz</td>
</tr>
<tr>
<td>STRATIX2 GX</td>
<td>-3</td>
<td>150/100</td>
<td>-</td>
<td>408 MHz</td>
</tr>
</tbody>
</table>

(Core performance in INTEL FPGA® devices)

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