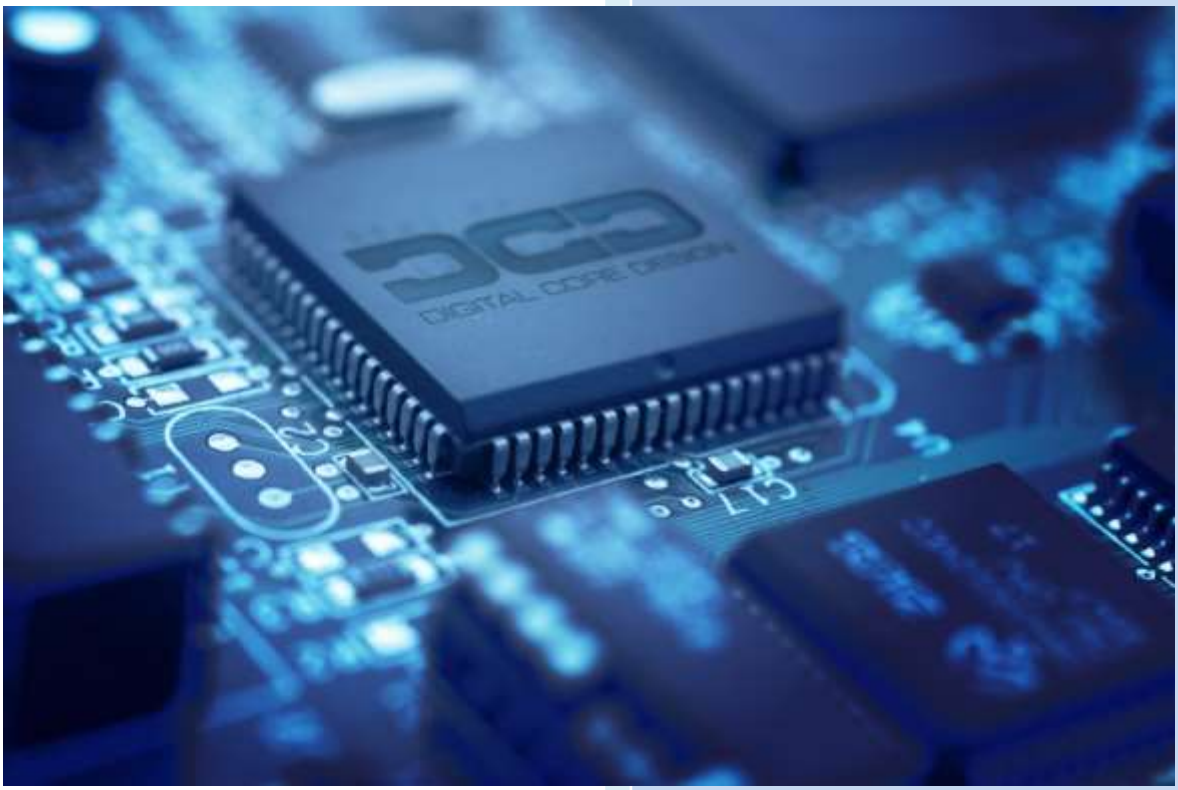
DIGITAL CORE DESIGN

2017

DBLCD32 IP Core



LCD/TFT Controller v. 2.00

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

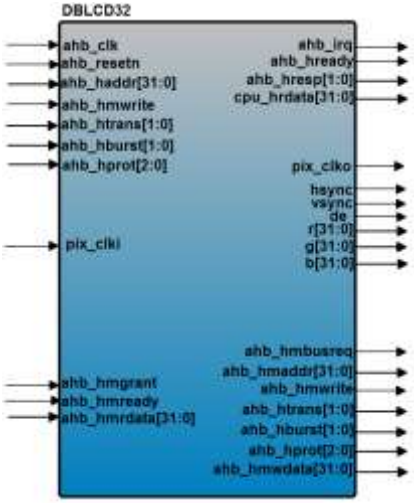
IP CORE OVERVIEW

The DCD's DBLCD32 core is a fully configurable, universal LCD/TFT display controller. It supports a wide range of resolution and enables both, horizontal and vertical synchronization parameters setup. The display's pixel clock can be generated by an internal pixel clock divider based on the bus clock, or delivered to the core by a dedicated pin. Additionally there is a possibility of using an externally generated pixel clock. Polarization of the generated pixel clock, as well as synchronization signals, is configurable. The DBLCD32 has a DMA capable master interface, which can be used to access a framebuffer placed directly in a system memory. Embedded DMA controller has configurable FIFO to store pixels data, which increases system throughput and performance. Transmission on the master interface is burst oriented and there is a possibility of defining the burst size limit. Data fetched by the DMA interface can be translated to 24-bits RGB signals, depending on the selected color mode. There are three standard color modes supported: 24-bits True Color, 16-bits(5-6-5) High Color and 8-bits index color mode. Additionally, a 32-bit True Color is also supported, but the MSB byte of each four byte word is ignored. In case of the Indexed Color Mode the DBLCD32 is equipped with pixel palette RAM which is used to translate each byte from the display buffer into 24-bit RGB output. There are two different formats of color palettes available. The core supports the page flipping mechanism, which enables the usage of multiple buffering totally without the tearing effect. There is also a set of programmable interrupts available related to both display synchronization and DMA status signals. The core is capable to work on both little and big endian systems. To increase the system performance and flexibility of usage, the DLBLCD32 can be configured in two possible optimization levels, to find a proper balance between a gate count and a critical path length.

FEATURES

- 24-bit RGB interface
- Configurable display resolution
- Configurable horizontal sync length and blanking
- Configurable vertical sync length and blanking
- Configurable RGB signals polarization
- Configurable pixel clock polarization
- Internal pixel clock divider
- Different pixel clock modes
- DMA capable interface
- Configurable DMA FIFO
- Configurable burst size limit
- AHB bus interface(32-bit)
- 24-bit True Color mode support
- 16-bit (5-6-5) High Color mode support
- 8-bit Indexed Color mode support
- 32-bit True Color mode support (one byte ignored)
- Pixel palette RAM
- Page flipping support
- Programmable interrupts
- Big and little-endian support
- Two different optimization levels
- Fully synthesizable, synchronous design

SYMBOL



UNITS SUMMARY

Registers – Module responsible of holding the configuration of the DBLCD32 as also providing interface to the status information and generating interrupts.

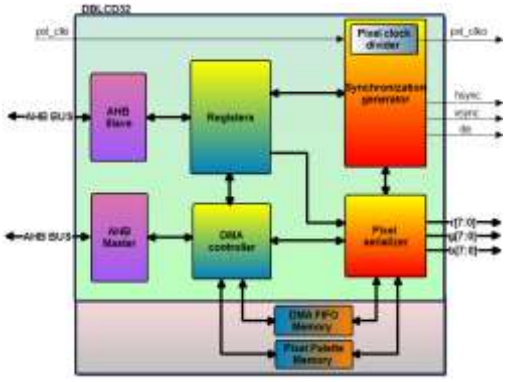
Synchronization generator – Generates synchronization signals and the pixel clock.

DMA controller – Fetches the framebuffer from the system memory and stores it in the DMA FIFO memory. When working in the indexed color mode it is also responsible of filling the Pixel Palette Memory.

Pixel serializer – Module responsible of serializing framebuffer data to the 24-bit RGB signaling depending of the chosen color mode. The pixel data is fetched from the DMA FIFO memory. When the index color mode **is** selected it uses Pixel Palette Memory to translate each byte to 24-bit RGB.

AHB Master, Slave – Wrappers to AMBA AHB interfaces.

BLOCK DIAGRAM



PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
AHB slave interface		
ahb_clk	Input	Bus clock
ahb_resetn	Input	BUS reset
ahb_haddr[31:0]	Input	The 32-bit system address bus
ahb_htrans[1:0]	Input	Type of the current transfer
ahb_hwrite	Input	Asserted indicates write transfer
ahb_hsize[2:0]	Input	Size of the transfer
ahb_hburst[2:0]	Input	Indicates if the transfer forms a part of a burst
ahb_hprot[3:0]	Input	Information about a bus access
ahb_hwdata[31:0]	Input	The write data bus
ahb_hsel	Input	Device select signal
ahb_hrdata[31:0]	Output	The read data bus
ahb_hresp[1:0]	Output	Information about a bus access.
ahb_irq	Output	Interrupt request
AHB master interface		
ahb_hrdata[31:0]	Input	The read data bus
ahb_hmgrant	Input	Indicates that the ownership of the bus
ahb_hmbusreq	Output	Indicates that the bus master requires the bus
ahb_hmaddr[31:0]	Output	The 32-bit system address bus
ahb_hmtrans[1:0]	Output	Indicates the type of the current transfer
ahb_hmwrite	Output	Asserted indicates write transfer
ahb_hmsize[2:0]	Output	Indicates the size of the transfer
ahb_hmprot[3:0]	Output	Information about a bus access
ahb_hmwdata[31:0]	Output	Information about a bus access
RGB Interface		
hsync	Output	Horizontal synchronization
vsync	Output	Vertical synchronization
de	Output	RGB data valid output
r[7:0]	Output	Red color data output bus
g[7:0]	Output	Green color data output bus
b[7:0]	Output	Blue color data output bus
Pixel clock Interface		
pxl_clki	Input	Pixel input clock
pxl_clko	Output	Pixel output clock

LICENSING

Comprehensible and clearly defined licensing methods **without royalty-per-chip fees** make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.

Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core:

- VHDL or Verilog RTL synthesizable HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM Netlist

DELIVERABLES

- Source code:
  - VERILOG Source Code or/and
  - VHDL Source Code or/and (optional)
  - FPGA Netlist
- VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - NCSim automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates, minor and major versions changes
    - Phone & email support

PERFORMANCE

The performance of the DBLCD32 is highly dependent on the used configuration. The tables below present **fully functional configurations,** however it is possible to disable some options to save the silicon area. Note that the given results are approximate, since the final implementation result depends on several external factors. All given area results are provided **without memory**. The tested **DMA FIFO memory** size is 256B. Additionally while using the **indexed color mode** the DBLCD32 has an internal **Pixel palette memory.** Its size is equal to 768B. The output pixel clock maximum frequency can be twice higher, without usage of the **Pixel clock divider**.

The following table gives a survey about the Core area and performance in INTEL FPGA® devices after Place & Route:

Device	ALMS/Registers	ahb_hclk / pxl_clko
ARIA V 5AGXFB3	270 / 360	248 MHz / 124 MHz
CYCLONE V 5CEBA9	268 / 365	168 MHz / 84 MHz
STRATIX V 5SEE9H	267/ 365	398 MHz / 199 MHz

Size optimized results. Pixel clock driven from the bus clock.

Device	ALMS/Registers	ahb_hclk / pxl_clko
ARIA V 5AGXFB3	295 / 399	370 MHZ / 200 MHz
CYCLONE V 5CEBA9	297 / 408	223 MHz / 114 MHz
STRATIX V 5SEE9H	323 / 400	564 MHz / 294 MHz

Speed optimized results. Pixel clock driven from the dedicated pin.

CONTACT

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