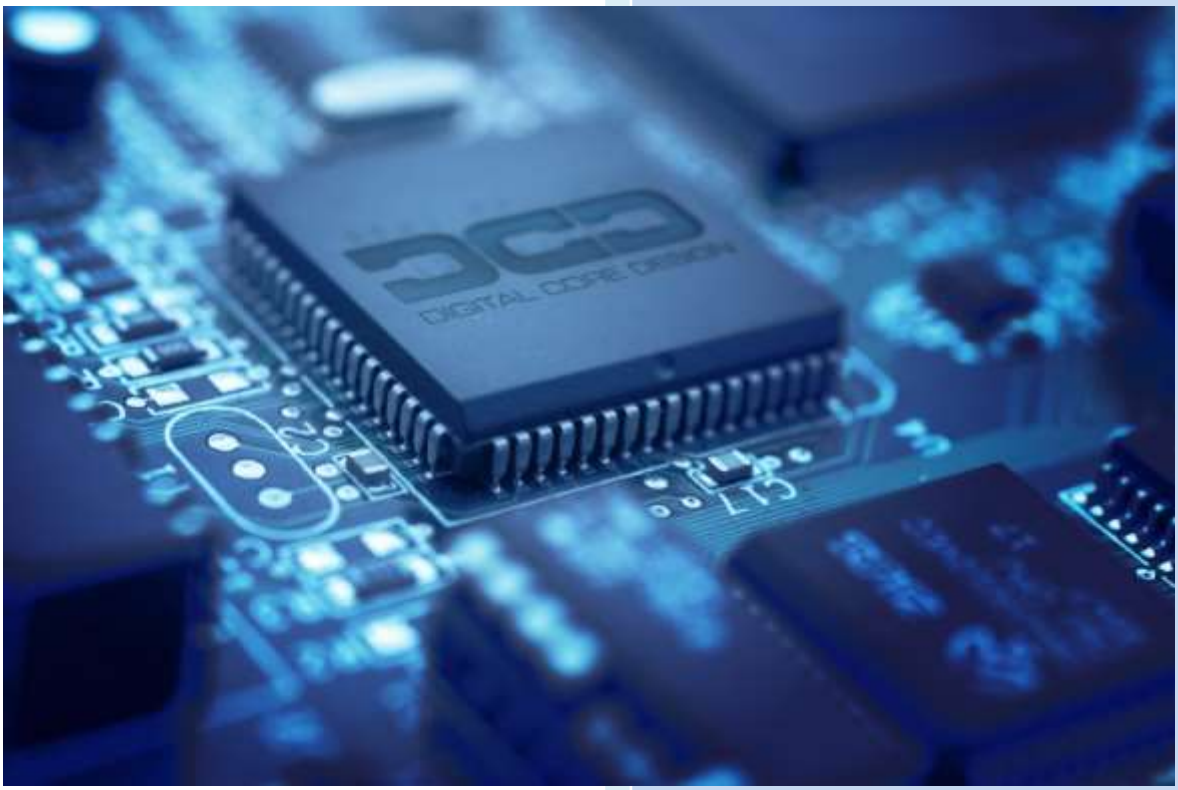
DIGITAL CORE DESIGN

2017

D16550 IP Core



Configurable UART with FIFO v. 2.25

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The D16550 is a soft Core of a Universal Asynchronous Receiver/Transmitter (UART), functionally identical to the TL16C550A. The D16550 allows serial transmission in two modes: UART and FIFO. In the FIFO mode, internal FIFOs are activated allowing 16 bytes (plus 3 bits of error data per byte in the RCVR FIFO) to be stored in both receive and transmit directions. The D16550 performs serial-to-parallel conversion on data characters, received from a peripheral device or a MODEM and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time, during the functional operation. Reported status information includes the type and condition of transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing or break interrupt). The D16550 includes a programmable baud rate generator, which is capable of dividing the timing reference clock input, by divisors of 1 to (2^{16}-1) and producing a 16 × clock, for driving the internal transmitter logic. Provisions are also included, to use this 16 × clock to drive the receiver logic. The D16550 has a complete MODEM control capability and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link. The separate BAUD CLK line allows setting an exact transmission speed, while the UART internal logic is clocked with the CPU frequency. There are two DMA modes supported: a single transfer and a multi-transfer. These modes allow the UART to interface to higher performance DMA units, which can interleave their transfers between CPU cycles or execute multiple byte transfers. The configuration capability allows the user to enable or disable during the synthesis process, the Modem Control Logic and FIFO's Control Logic, change the FIFO size. So, in applications with area limitation and where the UART works only in the 16450 mode, disabling Modem Control and FIFO's allows to save about 50% of logic resources. The D16550 has a universal microcontroller interface, which allows correct communication with the D16550, no matter how the D16550 clock is related to the microcontroller clock. The core is perfect for applications where the UART Core and microcontroller are clocked by the same clock signal and are implemented inside the same ASIC or FPGA chip. It also works well for a standalone implementation, where several UARTs are required to be implemented inside a single chip and driven by some off-chip devices. Thanks to the universal interface, the D16550 core implementation and verification are very simple, by eliminating a number of clock trees in complete system.

KEY FEATURES

- Software compatible with 16450 and 16550 UARTs
- Configuration capability
- Separate configurable BAUD clock line
- Two modes of operation: UART mode and FIFO mode
- Majority Voting Logic
- In the FIFO mode, transmitter and receiver are each buffered with 16 byte FIFO, to reduce the number of interrupts presented to the CPU
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to, or from the serial data
- In UART mode, receiver and transmitter are double buffered, to eliminate a need for precise synchronization between the CPU and serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- False start bit detection
- 16 bit programmable baud generator
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully programmable serial-interface characteristics:
  - *5-, 6-, 7-, or 8-bit characters*
  - *Even, odd, or no-parity bit generation and detection*
  - *1-, 1½-, or 2-stop bit generation*
  - *Baud generation*
- Complete status reporting capabilities
- Line break generation and detection. Internal diagnostic capabilities:
  - *Loop-back controls for communications link fault isolation*
  - *Break, parity, overrun, framing error simulation*
- Two DMA Modes allows single and multi-transfer
- Technology independent HDL Source Code
- Full prioritized interrupt system controls
- Fully synthesizable static design with no internal tri-state buffers

DESIGN FEATURES

The functionality of the D16550 core was based on the Texas Instruments' TL16C550A. The following characteristics differentiate the D16550 from Texas Instruments' devices:

- The bi-directional data bus have been split into two separate buses: datai (7:0), datao (7:0)
- Signals rd2 and wr2, xin and xout have been removed from interface
- Signal ADS and address latch have been removed
- The DLL, DLM and THR registers are reset to all zeros
- TEMT and THRE bits of Line Status Register, are reset during the second clock rising edge following a THR write
- RCLK clock is replaced by global clock CLK, internally divided by BAUD factor.
- Asynchronous microcontroller interface is replaced by equivalent Universal interface
- All latches implemented in original 16550 devices are replaced by equivalent flip-flop registers, with the same functionality

LICENSING

Comprehensible and clearly defined licensing methods **without royalty-per-chip fees** make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.

Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core:

- VHDL or Verilog RTL synthesizable HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM Netlist

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates, minor and major versions changes
    - Phone & email support

CONFIGURATION

The following parameters of the D16550 core can be easily adjusted to requirements of a dedicated application and technology. The configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

- Baud generator - enable / - disable
- External RCLK source - enable / - disable
- External BAUDCLK source - enable / - disable
- Modem Control logic - enable / - disable
- SCR Register - enable / - disable
- FIFO Control logic - enable / - disable

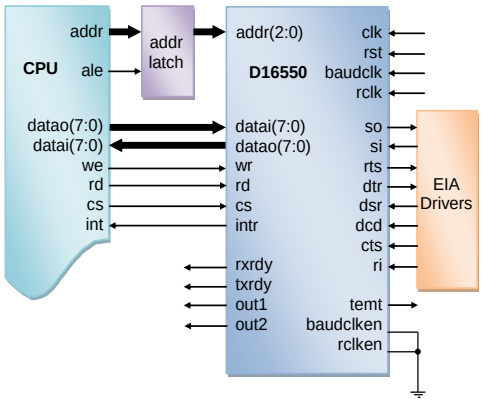
OPTIONAL FEATURES

- IEEE 1284 Bidirectional Parallel Data Port
  - *Compatible with Standard Centronics Parallel Interface*
  - *Support for Parallel Protocols: ECP and EPP*
  - *Decompression of Run Length Encoded Data in ECP Reserve Mode*
- Serial Ports with Infrared Data Association (IRDA) inputs and outputs

APPLICATIONS

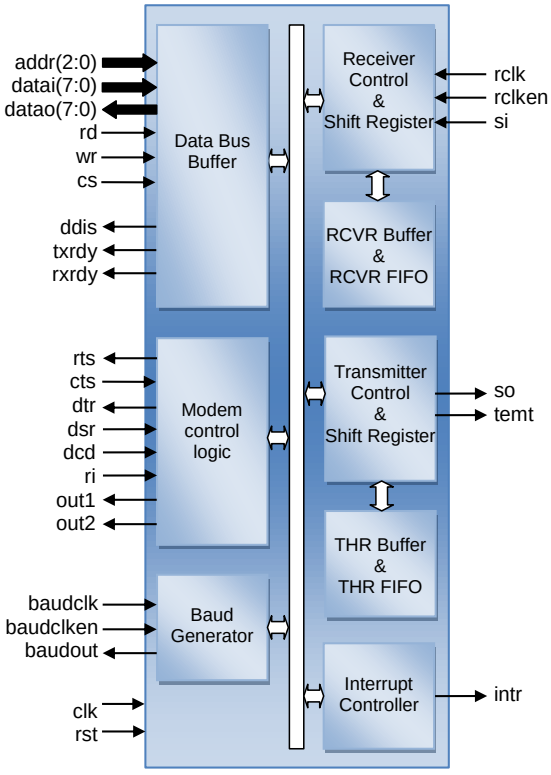
- Serial Data communications applications
- Modem interface

APPLICATION



Typical D16550 and processor connection is shown in the figure above.

BLOCK DIAGRAM



PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
rst	input	Global reset
clk	input	Global clock
datai[7:0]	input	Parallel data input
addr[2:0]	input	Address bus
cs	input	Chip select input
wr	input	Write input
rd	input	Read input
rclk	input	Receiver clock
baudclk	input	Baud generator clock
si	input	Serial data input
cts	input	Clear to send input
dsr	input	Data set ready input
dcd	input	Data carrier detect input
ri	input	Ring indicator input
baudclken	input	Baud generator clock enable
rclken	input	Receiver clock enable
baudout	output	Baud generator output
datao[7:0]	output	Parallel data output
so	output	Serial data output
ddis	output	Driver disable output
txrdy	output	Transmitter ready output
rxrdy	output	Receiver ready output
rts	output	Request to send output
dtr	output	Data terminal ready output
out1	output	Output 1
out2	output	Output 2
intr	output	Interrupt request output
temt	output	Transmitter empty

Note: When RCLK and BAUDCLK pins enabled, frequency should be at least two times lower than CLK, $2*f_{RCLK} < f_{CLK}$

UNITS SUMMARY

Baud Generator - The D16550 contains a programmable 16 bit baud generator that divides clock input by a divisor in the range between 1 and (2^{16}–1). The output frequency of the baud generator is 16 × the baud rate. The formula for the divisor is:

$$divisor = \frac{frequency}{baudrate * 16}$$

Two 8-bit registers, called divisor latches DLL and DLM, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the D16550, in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded on the CLK rising edge, following the write to DLL or DLM, to prevent long counts on initial load.

Data Bus Buffer - The data Bus Buffer accepts inputs from the system bus and generates control signals for other D16550 functional blocks. Address bus ADDR(2:0) selects one of the registers to be read from/written into. Both, RD and WE signals, are active low and are qualified by CS; RD and WE are ignored, unless the D16550 has been selected by holding CS low.

Modem Control Logic controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM).

Interrupt Controller - D16550 contains fully prioritized interrupt system controller. It controls interrupt requests to the CPU and interrupt priority. Interrupt controller contains Interrupt Enable (IER) and Interrupt Identification (IIR) registers.

Receiver Control - Receiving starts, when the falling edge on Serial Input (SI) during IDLE State is detected. After starting, the SI input is sampled every 16 internal baud cycles, as it is shown in figure above. When the logic 1 state is detected during START bit, it means, that the False Start bit was detected and receiver is back to the IDLE state.

Receiver FIFO - The Rx FIFO is 16 levels deep, it receives data, until the number of bytes in the FIFO, equals the selected interrupt trigger level. At that time, if R x interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes, until it holds 16 of them. It will not accept any more data, once it is full. Any more data entering the Rx shift register will set the Overrun Error flag.

Transmitter Control module controls transmission of written to THR (Transmitter Holding register) character via serial output SO. The new transmission starts on the next overflow signal of internal baud generator, after writing to THR register or Transmitter FIFO. Transmission control contains THR register and transmitter shift register.

Transmitter FIFO - the T x portion of the UART, transmits data through SO as soon as the CPU loads a byte into the T x FIFO. The UART will prevent loads to the T x FIFO, if it currently holds 16 characters. Loading to the T x FIFO will again be enabled, as soon as the next character is transferred to the T x shift register. These capabilities account for the largely autonomous operation of the T x. The UART starts the above operations typically with a T x interrupt.

DCD'S UART FAMILY OVERVIEW

The family of DCD's UART IP Cores combines high performance, low cost and a small compact size, offering best price/performance ratio in the IP Market. DCD's Cores are designed to be used in cost-sensitive consumer products, such as computer peripherals, office automation, automotive control systems, security and telecommunication applications. Our Cores are written in pure VHDL/VERILOG HDL languages, which makes them technologically independent. All DCD's UART IP Cores can be fully customized according to the customer's needs.

Design	SDLC	Synchronous Transmission	FIFO Size (Bytes)	Separate BAUD Clock I	Soft Flow Control – Xon/Xoff	RTS/CTS Flow Control	MODEM Control	False START detection	Complete status report	Internal diagnostic	Prioritized interrupts	Break gen. and detect	Half-Duplex RS485	IRDA Port	1284 Parallel Port
DUART	-	-	-	✓	-	-	-	✓	✓	✓	-	-	-	-	-
D2692	-	-	2*8	-	-	✓	-	✓	✓	✓	✓	✓	✓	-	-
D16450	-	-	-	✓	-	-	-	✓	✓	✓	✓	✓	-	-*	-*
D16550	-	-	2* 16	✓	-	-	-	✓	✓	✓	✓	✓	-	-*	-*
D16750	-	-	2* 64	✓	-	✓	✓	✓	✓	✓	✓	✓	*	*	*
D16552	-	-	2* 16	✓	-	-	-	✓	✓	✓	✓	✓	-	✓	✓
D16752	-	-	2* 64	✓	✓	✓	✓	✓	✓	✓	✓	✓	*	*	*
D16950	-	-	2* 128	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	*
D85C30	✓	✓	4	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	-	-

-Optional

PERFORMANCE

The following table gives a survey about the Core area and performance in INTEL FPGA® devices after Place & Route:

Device	Speed grade	Logic Cells	Memory Bits	F_{max}
ARIA GX	-6	342/231	304	243 MHz
ARIA V	-6	330/263	304	209 MHz
CYCLONE	-6	465	304	193 MHz
CYCLONE2	-6	476	304	220 MHz
CYCLONE3	-6	477	304	250 MHz
CYCLONE4	-6	478	304	250 MHz
CYCLONE5	-6	328/231	304	187 MHz
STRATIX	-5	465	304	206 MHz
STRATIX2	-3	342/232	304	343 MHz
STRATIX3	-2	334/231	304	527 MHz
STRATIX4	-2	330/250	304	497 MHz
STRATIX5	-2	332/262	304	456 MHz
STRATIX GX	-5	465	304	214 MHz
STRATIX2 GX	-3	340/231	304	341 MHz

Core performance in INTEL FPGA® devices

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