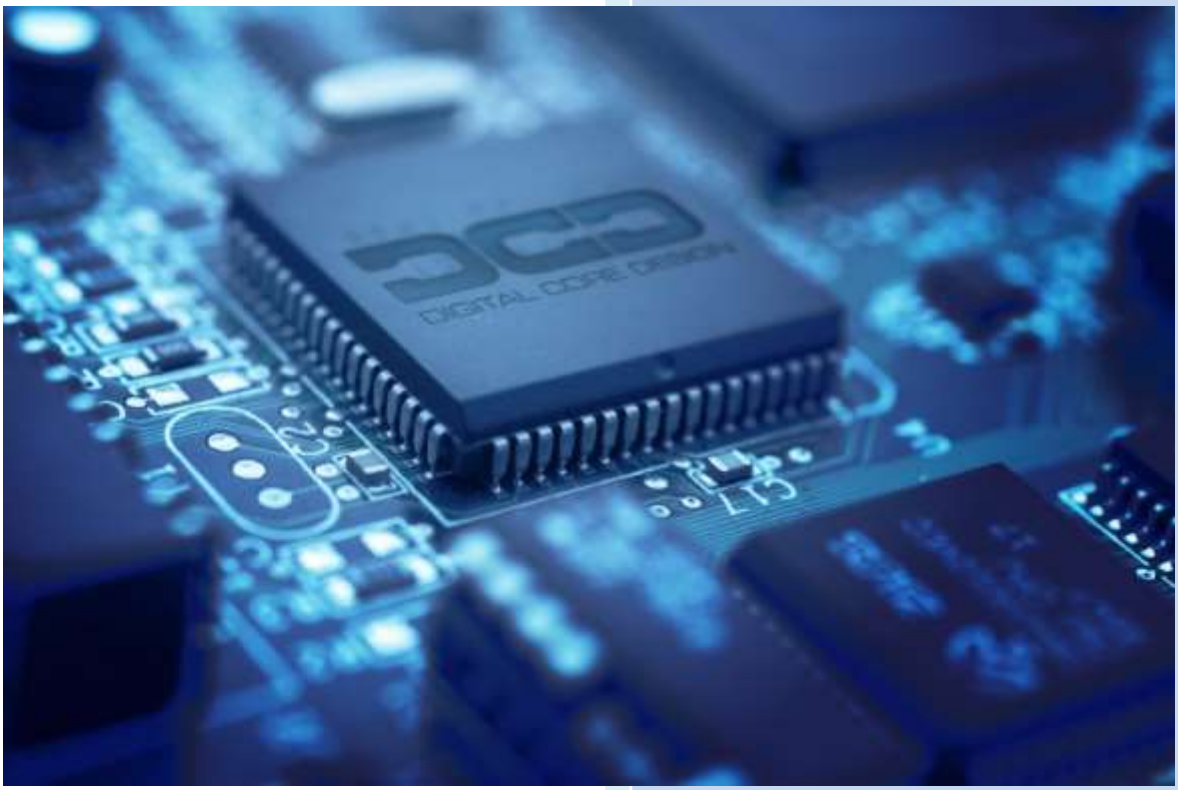
DIGITAL CORE DESIGN

2017

D16450 IP Core



Configurable UART v. 2.12

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The D16450 is a soft Core of a Universal Asynchronous Receiver/Transmitter (UART) functionally, identical to the TL16C450. The D16450 performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM; and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. The reported status information includes the type and condition of transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing or break interrupt). The D16450 includes a programmable baud rate generator, which is capable of dividing the timing reference clock input by divisors of 1 to (2^{16}-1) and producing a 16 × clock, for driving the internal transmitter logic. Provisions are also included to use this 16 × clock, to drive the receiver logic. The D16450 has a complete MODEM control capability and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link. A separate BAUD CLK line allows setting an exact transmission speed, while the UART internal logic is clocked with the CPU frequency. The core is perfect for applications, where the UART Core and a microcontroller are clocked by the same clock signal and are implemented inside the same ASIC or FPGA chip; as well as for a standalone implementation, where several UARTs are required to be implemented inside a single chip and driven by some off-chip devices. Thanks to the universal interface, the D16450 core implementation and verification are very simple, by eliminating a number of clock trees in a complete system.

KEY FEATURES

- Software compatible with the 16450 UART
- Configuration capability
- Separate configurable BAUD clock line
- Majority Voting Logic
- Adds or deletes standard asynchronous communication bits (start, stop, and parity), to or from the serial data
- In UART mode, receiver and transmitter are double buffered, to eliminate the need to precise synchronization between the CPU and serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- False start bit detection
- 16 bit programmable baud generator
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully programmable serial-interface characteristics:
  - *5-, 6-, 7-, or 8-bit characters*
  - *Even, odd, or no-parity bit generation and detection*
  - *1-, 1½-, or 2-stop bit generation*
- Complete status reporting capabilities
- Line break generation and detection. Internal diagnostic capabilities:
  - *Loop-back controls for communications link fault isolation*
  - *Break, parity, overrun, framing error*
- Technology independent HDL Source Code
- Full prioritized interrupt system controls
- Fully synthesizable static design with no internal tri-state buffers

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates, minor and major versions changes
    - Phone & email support

PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
rst	input	Global reset
clk	input	Global clock
datai[7:0]	input	Parallel data input
addr[2:0]	input	Address bus
cs	input	Chip select input
wr	input	Write input
rd	input	Read input
rclk	input	Receiver clock
baudclk	input	Baud generator clock
si	input	Serial data input
cts	input	Clear to send input
dsr	input	Data set ready input
dcd	input	Data carrier detect input
ri	input	Ring indicator input
baudclken	input	Baud generator clock enable
rclken	input	Receiver clock enable
baudout	output	Baud generator output
datao[7:0]	output	Parallel data output
so	output	Serial data output
ddis	output	Driver disable output
rts	output	Request to send output
dtr	output	Data terminal ready output
out1	output	Output 1
out2	output	Output 2
intr	output	Interrupt request output

DESIGN FEATURES

The functionality of the D16450 core was based on the Texas Instruments' TL16C450. The following characteristics differentiate the D16450 from Texas Instruments' devices:

- The bi-directional data bus has been split into two separate buses: datai(7:0), datao(7:0)
- Signals rd2 and wr2, xin, and xout have been removed from interface
- Signal ADS and address latch have been removed
- The DLL, DLM and THR registers are reset to all zeros
- TEMT and THRE bits of Line Status Register, are reset during the second clock rising edge, following a THR write
- RCLK clock is replaced by global clock CLK, internally divided by BAUD factor.
- Asynchronous microcontroller interface is replaced by equivalent Universal interface
- All latches implemented in original 16450 devices are replaced by equivalent flip-flop registers with the same functionality

LICENSING

Comprehensible and clearly defined licensing methods **without royalty-per-chip fees** make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.

Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core:

- VHDL or Verilog RTL synthesizable HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM Netlist

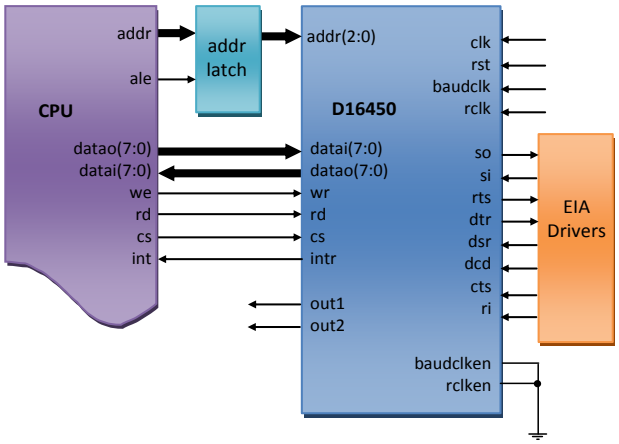
CONFIGURATION

The following parameters of the D16450 core can be easily adjusted to requirements of a dedicated application and technology. Configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

- Baud generator - enable / - disable
- External RCLK source - enable / - disable
- External BAUDCLK source - enable / - disable
- Modem Control logic - enable / - disable
- SCR Register - enable / - disable

Note: When enabled RCLK and BAUDCLK pins frequency should be at least two times lower than CLK, $2*f_{RCLK} < f_{CLK}$

APPLICATION



UNITS SUMMARY

Data Bus Buffer - The data Bus Buffer accepts inputs from the system bus and generates control signals for other D14750 functional blocks. Address bus ADDR(2:0) selects one of the register to be read from/written into. Both, RD and WE signals, are active low and are qualified by CS; RD and WE are ignored, unless the D16450 has been selected by holding CS low.

Baud Generator - The D16450 contains a programmable 16 bit baud generator that divides clock input by a divisor, in the range between 1 and (2^{16}–1). The output frequency of the baud generator is 16 × the baud rate. The formula for the divisor is:

$$divisor = \frac{frequency}{baudrate * 16}$$

Two 8-bit registers, called divisor latches DLL and DLM, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the D16450, in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded on the CLK rising edge, following the write to DLL or DLM, to prevent long counts on initial load.

Modem Control Logic controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM).

Interrupt Controller - D16450 contains a fully prioritized interrupt system controller. It controls interrupt requests to the CPU and interrupt priority. Interrupt controller contains Interrupt Enable (IER) and Interrupt Identification (IIR) registers.

Receiver Control – The receiving starts, when the falling edge on Serial Input (SI) during IDLE State is detected. After starting the SI input is sampled every 16 internal baud cycles, as it is shown in the figure below. When the logic 1 state is detected during START bit, it means, that the False Start bit was detected and receiver back to the IDLE state.

Transmitter Control module controls transmission of written to THR (Transmitter Holding register) character via serial output SO. The new transmission starts on the next overflow signal of internal baud generator, after writing to THR register or Transmitter FIFO. Transmission control contains THR register and transmitter shift register.

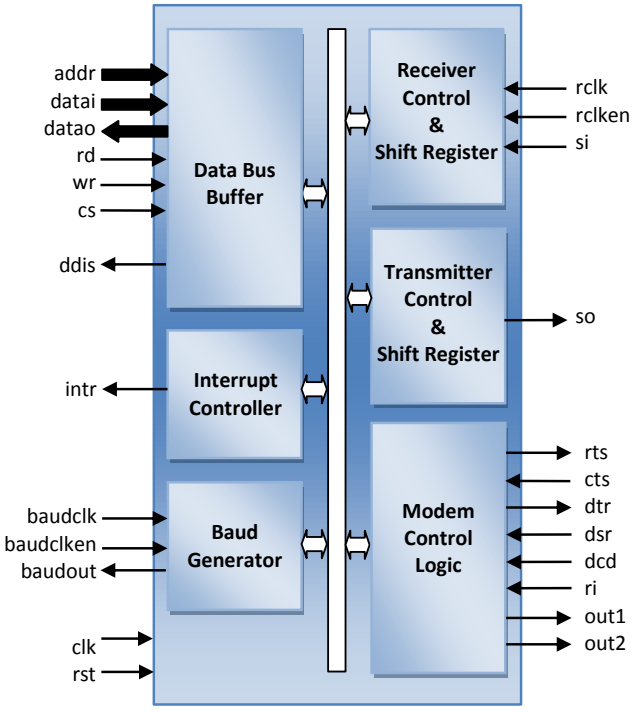
DCD'S UART FAMILY OVERVIEW

The family of DCD's UART IP Cores combines high performance, low cost and a small compact size, offering best price/performance ratio in the IP Market. DCD's Cores are designed to be used in cost-sensitive consumer products, such as computer peripherals, office automation, automotive control systems, security and telecommunication applications. Our Cores are written in pure VHDL/VERILOG HDL languages, which makes them technologically independent. All DCD's UART IP Cores can be fully customized according to the customer's needs.

Design	SDLC	Synchronous Transmission	FIFO Size (Bytes)	Separate BAUD Clock I	Soft Flow Control – Xon/Xoff	RTS/CTS Flow Control	MODEM Control	False START detection	Complete status report	Internal diagnostic	Prioritized interrupts	Break gen. and detect	Half-Duplex RS485	IRDA Port	1284 Parallel Port
DUART	-	-	-	✓	-	-	-	✓	✓	✓	-	-	-	-	-
D2692	-	-	2*8	-	-	✓	-	✓	✓	✓	✓	✓	✓	-	-
D16450	-	-	-	✓	-	-	-	✓	✓	✓	✓	✓	-	-*	-*
D16550	-	-	2* 16	✓	-	-	-	✓	✓	✓	✓	✓	-	-*	-*
D16750	-	-	2* 64	✓	-	✓	✓	✓	✓	✓	✓	✓	*	*	*
D16552	-	-	2* 16	✓	-	-	-	✓	✓	✓	✓	✓	-	✓	✓
D16752	-	-	2* 64	✓	✓	✓	✓	✓	✓	✓	✓	✓	*	*	*
D16950	-	-	2* 128	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	*
D85C30	✓	✓	4	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	-	-

***-Optional**

BLOCK DIAGRAM



PERFORMANCE

The following table gives a survey about the Core area and performance in INTEL FPGA® devices, after Place & Route:

Device	Speed grade	Logic Cells	F_{max}
CYCLONE	-6	301	190 MHz
CYCLONE 2	-6	303	222 MHz
STRATIX	-5	301	213 MHz
STRATIX 2	-3	248	283 MHz
STRATIXGX	-5	301	212 MHz
MERCURY	-5	350	222 MHz
EXCALIBUR	-1	340	137 MHz
APEX II	-7	340	145 MHz
APEX20KC	-7	340	143 MHz
APEX20KE	-1	340	122 MHz
APEX20K	-1	340	83 MHz
ACEX1K	-1	363	99 MHz
FLEX10KE	-1	363	98 MHz

Core performance in INTEL FPGA® devices

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