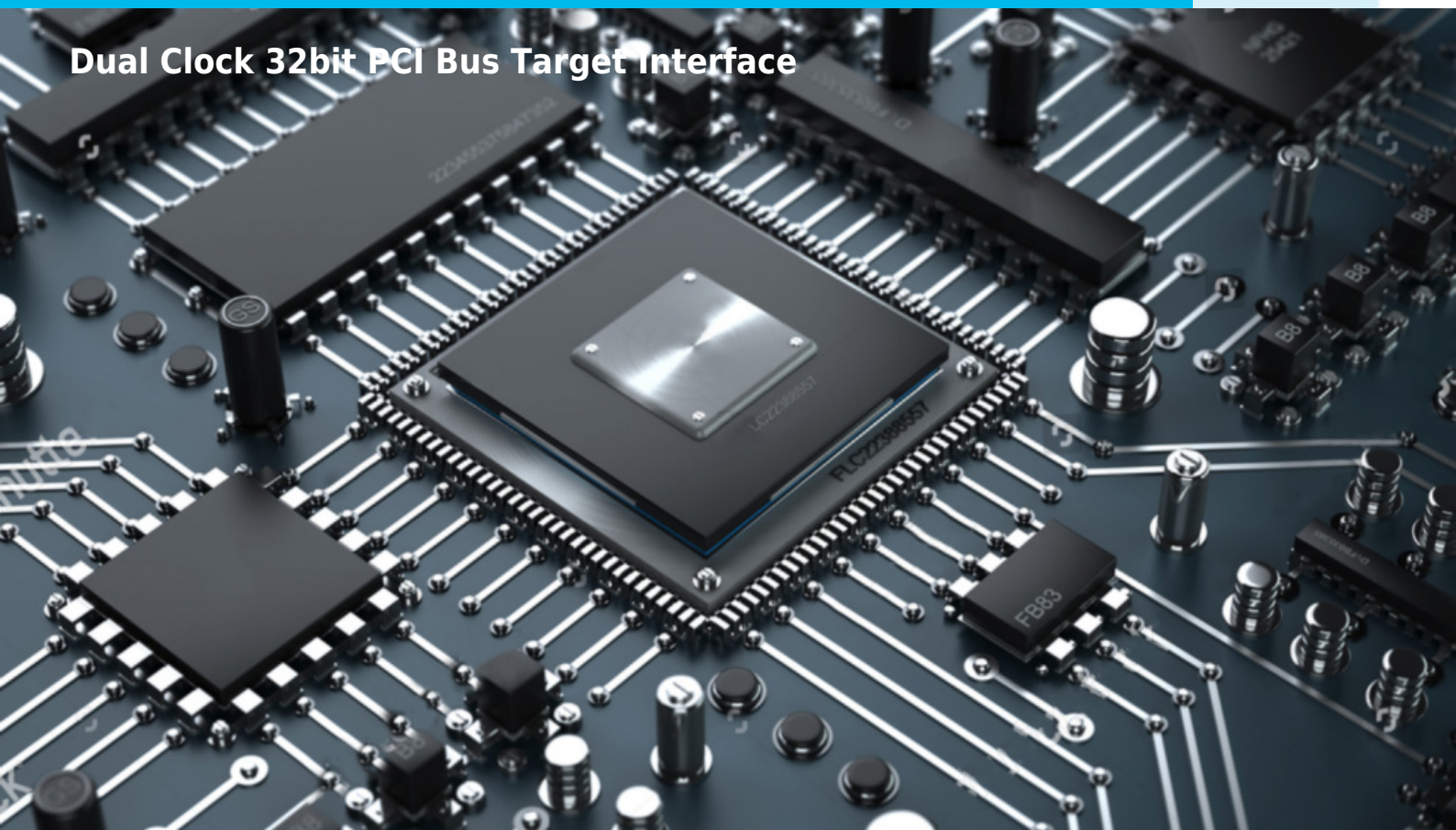
DIGITAL CORE DESIGN

DTPCI32DC

Dual Clock 32bit PCI Bus Target Interface



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DTPCI32DC is a 32-bit target interface which provides **all requirements of the PCI 3.0 specification** for a target device. It compromises a minimal gate count with a high-bandwidth data transfer. The Core's main feature is a **presence of two clock domains** which enable flexibility as well as higher performance. When time required for implementation becomes crucial, the **DTPCI32DC brings domain crossing**. The time saved can be used for a specific system implementation instead. The user-friendly back-end interface can be very easily and effectively tailored to the design needs. The Core **supports up to six Base Address Registers** and **Expansion Rom address register** with **both I/O and Memory space decoding from 16 bytes up to 4 GB**. Another important feature is a **cache wrapping hardware support** and **cacheline pre-fetching capability**. The DTPCI32DC is accepting size cache lines which are powered from 2 up to 128. It enables also **target-disconnect** with data, without data or by target abort. Moreover, the DTPCI32DC is able to **work with 66 MHz clock frequency** in most popular technologies. It assures PCI timing requirements as well as other parameters, like FIFOs depths number and Base Address Registers (they can be easily configured at the pre-synthesis stage).

KEY FEATURES

- Fully supports PCI specification 3.0 protocol
- Stable clock domain crossing regardless of the clock frequencies
- Cache wrapping (cache lines must be powers of 2)
- User controlled burst data transfer
- Possible no-wait state transactions
- Automatic handling of configuration space read/write access
- Parity generation and parity error detection
- Single interrupt support
- Configurable FIFOs depth
- Supported backend initiated burst termination (with and without data)
- No tri-state buffers

UNITS SUMMARY

Configuration space – Holds information about status of the DTPCI32DC and also controls its behavior. CS contains the base address registers which encode the addressing spaces and sizes.
Address Decoder – Responsible for decoding the addresses which have been previously written into the base address registers in the configuration space. This module provides also cache line wrapping decoding.
Command decoder – Responsible for decoding to the control flags which are encoded in the PCI_CBE strobe.
Parity module – Generates the parity and checking if the parity input matches the calculated value and also parity and system error generation.
Synchronizers – Their role is to synchronize internal and external signals to the "opposite" clock domain.
Incoming and Outgoing FIFO controllers – Responsible for synchronization of data between the domains. The pointers of FIFOs are encoded in the **grey code**.
Back-end controller – Responsible for the back-end address generation and also cache wrapping and cacheline prefetching.

APPLICATIONS

The DTPCI32DC offers a highly customizable and scalable solution, designed to meet the requirements of various applications.

PERFORMANCE

The table below gives general information about the area size and maximum clock frequency of the DTPCI32DC. Beware that the area size may vary a lot between the configurations. That's why below results present rough estimations based on DCD's testing platform. The value of the maximum PCI clock frequency is omitted, because the PCI interface can work with two possible clock frequencies: 33 MHz and 66 MHz. All cell numbers are presented without memories. The synthesis strategy is balanced. The maximum frequencies are given for the minimal version. For more detailed information about performance please contact DCD.

Device	Cell min LE/ALM	Cell full LE/ALM	BEND Fmax
Arria II GX	295/176	500/324	398
Arria V	167/177	338/326	297
Cyclone IV GX	355/176	707/324	250
Cyclone V	168/176	335/326	213
MAX 10	357/176	716/324	207
Stratix IV	295/176	502/324	469
Stratix V	167/178	336/328	497

Core performance in INTEL FPGA® devices

DELIVEVERABLES

- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates, minor and major versions changes
    - Phone & email support

LICENSING

Transparent and clearly defined licensing methods without royalty-per-chip fees, make use of our IP Cores easy & simple.
– ***Single-Site license option*** – dedicated to small and middle sized companies, which run their business in one place.
– ***Multi-Site license option*** – dedicated to corporate customers who operate at several locations. The licensed product can be used in selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.
There are two formats of the delivered IP Core:
– VHDL or Verilog RTL synthesizable HDL Source code
– FPGA EDIF/NGO/NGD/QXP/VQM Netlist

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