



2017

DT8051 IP Core



Tiny Area 8051-compatible Microcontroller v. 4.71

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DT8051 is an **area optimized**, tiny soft core, of a single-chip 8-bit embedded microcontroller, based on World's fastest and most popular DP8051 core, available since over 8 years. The DT8051 soft core is 100% binary-compatible with the industry standard 8051 8-bit microcontroller. It has a very low gate count architecture, giving 6 650 ASIC gates for a complete system, including the DoCD on-chip debugger. **Dhrystone 2.1 benchmark program runs exactly 8.1 times faster than the original 80C51** at the same frequency. The same C compiler was used for benchmarking of the core vs. 80C51, with the same settings. The DT8051 Core has a built-in support for the 2-wire TTAG™ interface - DCD Hardware Debug System, called **DoCD™**. This version of the debugger is dedicated for applications, where a number of external pins is limited. The DT8051 includes also up to eight external interrupt sources, an advanced Power Management Unit, Timers 0&1, I/O bit addressable Ports, a full duplex UART and an interface for external SFR. It is delivered with **fully automated test bench** and **complete set of tests**, allowing easy package validation at each stage of SoC design flow.

KEY FEATURES

- Software compatible with the 8051 industry standard
- Very low gate count, area optimized architecture – 6 650 ASIC gates for a **complete system** with DoCD on-chip debugger
- 8.1 times faster than a standard 8051
- 7.63 VAX MIPS at 100 MHz
- Up to 256 bytes of internal (on-chip) Data Memory
- Up to 64k bytes of internal (on-chip) Program Memory
- Up to 64k bytes of external (off-chip) Program Memory
- Up to 64k bytes of external (off-chip) Data Memory
- De-multiplexed Address/Data Bus to allow easy connection to memory
- Power Management Unit
 - *Power management mode*
 - *Switchback feature*
 - *Stop mode*
- Interrupt Controller
 - *2 priority levels*
 - *8 external interrupt sources*
 - *3 interrupt sources from peripherals*
- 8-bit I/O Port
 - *Bit addressable data direction for each line*

- *Read/write of single line and 8-bit group*
- Two 16-bit timer/counters
 - *Timers clocked by internal source*
 - *Auto reload 8-bit timers*
 - *Externally gated event counters*
- Full-duplex serial port
 - *8-bit asynchronous mode, variable baud rate*
 - *9-bit asynchronous mode, variable baud rate*
- Interface for additional Special Function Registers
- **2-wire DoCD™** debug unit
 - *Processor execution control*
 - *Run, Halt*
 - *Step into instruction*
 - *Skip instruction*
 - *Read-write all processor contents*
 - *Program Counter (PC)*
 - *Program Memory*
 - *Internal (direct) Data Memory*
 - *Special Function Registers (SFRs)*
 - *External Data Memory*
 - *Code execution breakpoints*
 - *two real-time PC breakpoints*
 - *unlimited number of real-time OPCODE breakpoints*
 - *Three independent Memory watchpoints*
 - *SFR, DATA, XDATA*
 - *2-wire TTAG communication interface*
- Fully synthesizable, static synchronous design, with positive edge clocking and no internal tri-states
- Scan test ready

DELIVERABLES

- ♦ Source code:
 - VHDL Source Code or/and
 - VERILOG Source Code or/and
 - Encrypted, or plain text EDIF
- ♦ VHDL & VERILOG test bench environment
 - Active-HDL automatic simulation macros
 - ModelSim automatic simulation macros
 - Tests with reference responses
- ♦ Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
- ♦ Synthesis scripts
- ♦ Example application
- ♦ Technical support
 - IP Core implementation support
 - 3 months maintenance
 - Delivery of the IP Core and documentation updates, minor and major versions changes
 - Phone & email support

APPLICATIONS

- ♦ Low power battery operated devices
- ♦ Mixed signal systems
- ♦ Area optimized FPGA/ASIC design
- ♦ FSM replacements

BENEFITS

- ♦ Lowest gate count, 8051 compatible architecture
- ♦ Very low power consumption
- ♦ Significant performance improvement with respect to the 80C51 device, working at the same clock frequency (**8.1 in terms of Dhrystone MIPS**)
- ♦ On demand customization

PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
port2i[7:0]	input	Port 2 input
prgdatai[7:0]	input	Data bus from internal program memory
xdatai[7:0]	input	Data bus from external data/code memory
ramdatai[7:0]	input	Data bus from internal data memory
sfrdatai[7:0]	input	Data bus from user SFR's
int0	input	External interrupt 0
int1	input	External interrupt 1
int2	input	External interrupt 2
int3	input	External interrupt 3
int4	input	External interrupt 4
int5	input	External interrupt 5
int6	input	External interrupt 6
int7	input	External interrupt 7
t0	input	Timer 0 input
t1	input	Timer 1 input
gate0	input	Timer 0 gate input
gate1	input	Timer 1 gate input
rxdi	input	Serial receiver input
ttidi	input	DoCD data input
port2o[7:0]	output	Port 2 output
prgaddr[15:0]	output	Internal program memory address bus
prgdatao[7:0]	output	Data bus for Internal program memory
prgramwr	output	Internal program memory write
address[15:0]	output	External data/code memory address bus
xdatao[7:0]	output	Data bus for external data/code memory
xdataz	output	External XDATA bus 'Z' state
xdatawr	output	External data memory write
xdatard	output	External data memory read
xprgrd	output	External program memory read
xprgwr	output	External program memory write
ramaddr[7:0]	output	RAM address bus
ramdatao[7:0]	output	Data bus for internal data memory
ramwe	output	Internal data memory write enable
ramoe	output	Internal data memory output enable
sfraddr[6:0]	output	SFR's address bus
sfrdatao[7:0]	output	Data bus for user SFR's
sfrwe	output	User SFR's write enable
sfroe	output	User SFR's output enable
txd	output	Serial transmitter output
ttck	output	DoCD clock output
ttdoen	output	DoCD data output enable
ttdo	output	DoCD data output

UNITS SUMMARY

ALU - Arithmetic Logic Unit - performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic, like arithmetic unit, logic unit, multiplier and divider.

Control Unit - It performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and manages execution of all microcontroller tasks.

Program Memory Interface - It contains Program Counter (PC) and related logic. It performs the instructions code fetching. Whole program memory (FLASH or SRAM type), can be written by DoCD™ debugger or application can modify some part of its code - for example, storing some data which shouldn't volatile.

External Memory Interface - Contains memory access related registers, like Data Page High (DPH) and Data Page Low (DPL) registers. It performs the memory addressing and data transfers.

Internal Data Memory Interface - Interface controls access into the internal memory of size up to 256 bytes. It contains 8-bit Stack Pointer (SP) register and related logic.

SFR's Interface - Special Function Register interface, manages communication between CPU and user specified special registers.

Opcode Decoder - Performs an opcode decoding instruction and control functions for all other blocks.

Interrupt Controller - Interrupt Control module is responsible for the interrupt manage system for the eight external and internal interrupt sources. It contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IP), Extended Interrupt Enable (EIE), Extended Interrupt priority (EIP) and (TCON) registers.

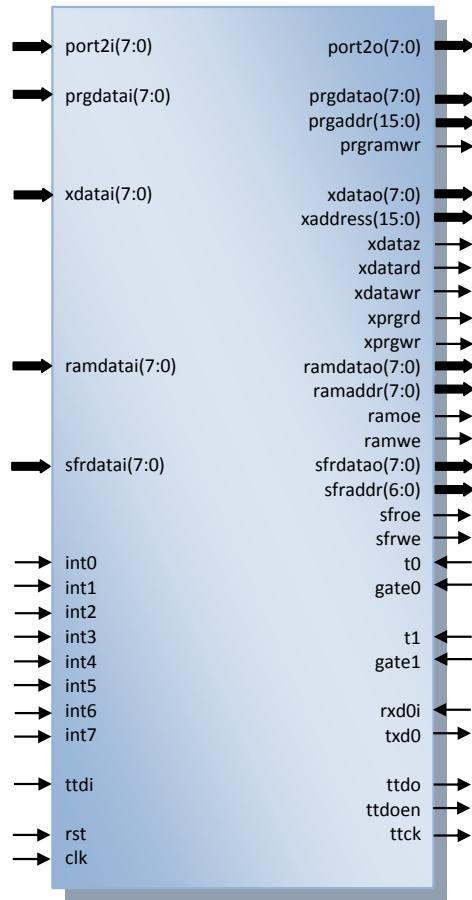
Timers - System timers module. Contains two 16bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 (or 4) CLK periods, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.

UART - Universal Asynchronous Receiver & Transmitter module is full duplex, meaning, it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, so it can commence reception of a second byte before the previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register, and reading SBUF0, reads a physically separate receive register. It works in 2 asynchronous modes with variable baud rate, covering all standard transmission speeds.

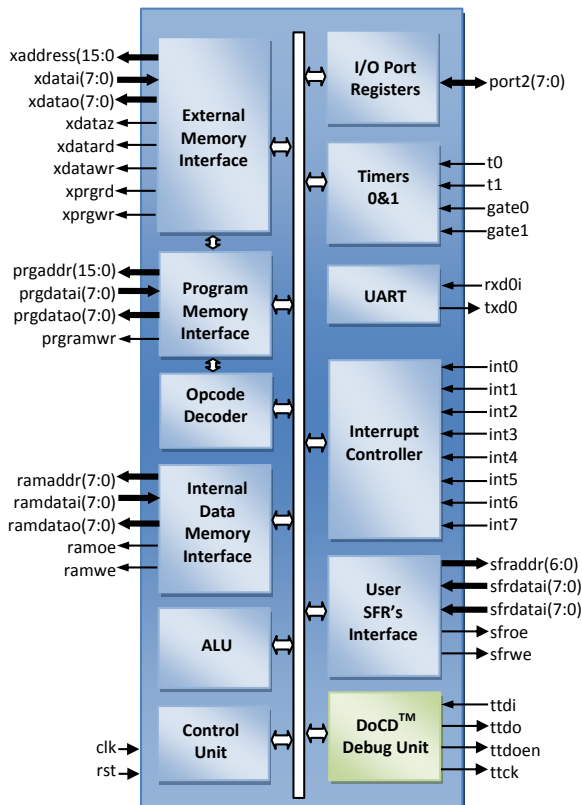
Ports - Block contains 8051's general purpose I/O ports. Each of port's pin can be read/write as a single bit or as an 8-bit bus.

DoCD™ Debug Unit – it is a DoCD™ Debug Unit, **2-wire, low gate count, real-time hardware debugger**, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, DoCD™ provides **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints control execution of program memory code; hardware watchpoints can be set and control internal and external data memories and SFRs. Hardware watchpoints are executed if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins (CODERUN and DEBUGACS) indicate the state of the debugger and CPU. CODERUN is active, when CPU is executing an instruction. DEBUGACS pin is active, when any access is performed by DoCD™ debugger. The DoCD™ system includes **TTAG interface** and complete set of tools, to communicate and work with core, in real time debugging. It is built as scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off.

SYMBOL



BLOCK DIAGRAM



LICENSING

Comprehensible and clearly defined licensing methods **without royalty-per-chip fees** make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.

Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core:

- VHDL or Verilog RTL synthesizable HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM Netlist

PERFORMANCE

The following tables give a survey about the DT8051 and the DoCD on-chip debugger area and performance in the most popular ASIC technologies (all features are included). Results given for working system with connected SFR IDATA, CODE and XDATA memories.

Technology / optimization	Speed grade	Area [gates]	F _{max}
0.25u area	typical	6 000	100 MHz
0.18u area	typical	5 720	130 MHz
0.09u area	typical	5 600	230 MHz

DT8051 without DoCD debugger

Technology / optimization	Speed grade	Area [gates]	F _{max}
0.25u area	typical	7 530	100 MHz
0.18u area	typical	7 150	130 MHz
0.09u area	typical	6 650	230 MHz

DT8051 with compact version¹ of DoCD debugger

Technology / optimization	Speed grade	Area [gates]	F _{max}
0.25u area	typical	8 150	100 MHz
0.18u area	typical	7 720	130 MHz
0.09u area	typical	7 300	230 MHz

DT8051 with full version² of DoCD debugger

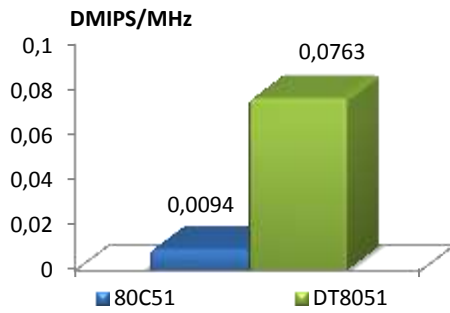
1- compact DoCD version includes processor execution control (*run, halt, reset, step*); read-write all processor content (*PC, SFRs*); read-write all processor memories (*IDATA, XDATA, CODE memory*); FLASH code memory programming; one hardware code execution breakpoint; unlimited number of OPCODE execution breakpoints

2- full DoCD version includes processor execution control (*run, halt, reset, step*); read-write all processor content (*PC, SFRs*); read-write all processor memories (*IDATA, XDATA, CODE memory*); FLASH CODE memory programming; two hardware code execution breakpoints; six configurable hardware watch-points (*IDATA, XDATA, SFRs*); unlimited number of OPCODE execution breakpoints

Dhrystone Benchmark Version 2.1 was used, to measure the Core performance. The following table gives a survey about the DT8051 performance, in terms of Dhrystone/sec and VAX MIPS rating per 1 MHz (DMIPS/MHz).

Device	Dhry/sec [12 MHz]	DMIPS/MHz	80C51 ratio
80C51	197	0,0094	1,00
DT8051	1597	0,0763	8,11

DT8051 performance in terms of DMIPS/MHz



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