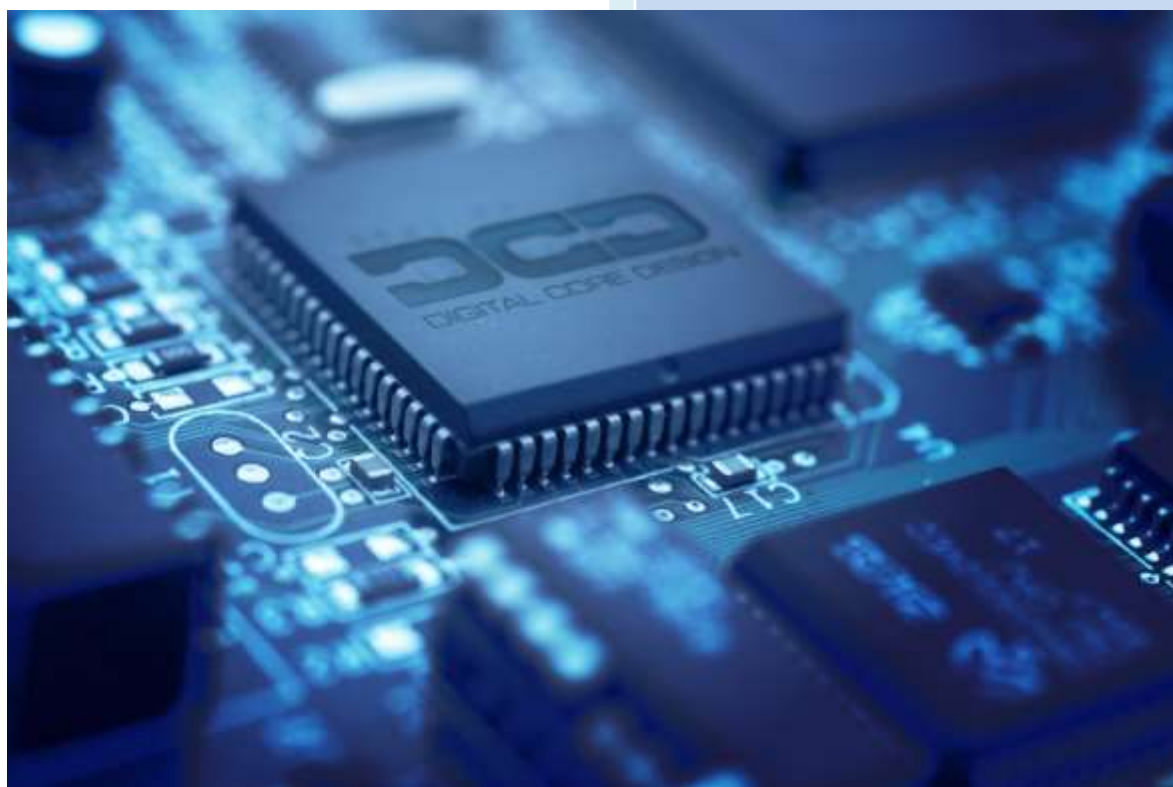




2017

DQ80251 IP Core



Revolutionary Quad-Pipelined Ultra High Performance 16/32-bit Configurable
Microcontroller v. 6.06

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DQ80251 is a revolutionary **quad-pipelined ultra-high performance, speed optimized** soft core, of a 16-bit/32-bit embedded microcontroller. **The core is fully configurable** and allows selection of its features and peripherals, to create a dedicated system. The core has been designed with a special concern of performance to power consumption ratio. This ratio is extended by an **Advanced Power Management Unit – the PMU**. This product was built based on 14 years of DCD's know-how with triumphant 8051 architectures. The DQ80251 soft core is 100% binary-compatible with the 16-bit 80C251 and 8-bit 80C51 industry standard microcontrollers. There are two working modes of the DQ80251: **BINARY** (where the original 80C51 compiled code is executed) and **SOURCE** (a native 80C251 mode, using all DQ80251 performance). The DQ80251 has a built-in, configurable DoCD-JTAG on-chip debugger, supporting Keil DK251 and standalone DoCD debug software. **Dhrystone 2.1 benchmark program runs 66 times faster than the original 80C51 and 5.5 times faster, than the original 80C251 at the same frequency.** This performance can be also exploited to great advantage in **low power** applications, where the core can be clocked over fifty times slower than the original implementation, with no performance penalty. Additionally, a compiled code size for the SOURCE mode is about **2 times smaller** comparing to the standard 8051 code, since DQ80251 instructions are more effective. The DQ80251 is delivered with **fully automated test bench** and **complete set of tests**, allowing easy package validation at each stage of SoC design flow.

CPU FEATURES

- 100% binary compatible with the 80C251 industry standard, implementing BINARY and SOURCE modes
- Single clock period per most of instructions
- **Quad-Pipelined** architecture enables to run **66 times faster** than the original 80C51 and **5.5 times faster** than the 80C251 at the same frequency
- Up to **61.8 VAX MIPS** at 100 MHz
- Up to 8M bytes of Program Memory
- Up to 32k bytes of internal (on-chip) Data Memory
- Up to 8M bytes of external (off-chip) Data Memory
- Up to 16 MB of total memory space for CODE and DATA
- 32k bytes of extended stack space

- User programmable Program Memory Wait States solution for wide range of memories speed
- User programmable Extended Data Memory Wait States solution for wide range of memories speed
- De-multiplexed Address/Data bus to allow easy connection to memory
- Full Program Memory writes
- Interface for additional Special Function Registers
- Fully synthesizable, static synchronous design with positive edge clocking and no internal tri-states
- Scan test ready

DESIGN FEATURES

◆ PROGRAM MEMORY:

The DQ80251 is dedicated for operation with Internal and External Program Memory up to 8MB of size. It can be configured as synchronous or asynchronous.

◆ DATA MEMORY:

The DQ80251 can address synchronous Internal Data Memory of up to 32k bytes and up to 8MB of External Data Memory. The External Data Memory interface can be configured as synchronous or asynchronous. XDATA memory (from 8051/ 80390) is inside the EDATA space.

◆ USER SPECIAL FUNCTION REGISTERS:

Up to 60 External (user) Special Function Registers (ESFRs) may be added to the DQ80251 design. ESFRs are memory mapped into Direct Memory between addresses 0x80 and 0xFF, in the same manner, as core SFRs and may occupy any address which is not occupied by a core SFR.

◆ WAIT STATES SUPPORT:

The DQ80251 soft core is dedicated for operation with wide range of Program and Data memories. Slow Program and Extended Data memory may assert memory WAIT signals, to hold up CPU activity for required period of time.

DELIVERABLES

- ◆ Source code:
 - VHDL Source Code or/and
 - VERILOG Source Code or/and
 - Encrypted, or plain text EDIF
- ◆ VHDL & VERILOG test bench environment
 - Active-HDL automatic simulation macros
 - ModelSim automatic simulation macros
 - Tests with reference responses
- ◆ Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - IP Core implementation support
 - 3 months maintenance
 - Delivery of the IP Core and documentation updates, minor and major versions changes
 - Phone & email support

PERIPHERALS

- **DoCD™ debug unit**
 - Processor execution control
 - Run, Halt
 - Step into instruction
 - Skip instruction
 - Read-write all processor contents
 - Program Counter (PC)
 - Program Memory
 - Internal (direct) Data Memory
 - Special Function Registers (SFRs)
 - Extended Data Memory
 - Code execution breakpoints
 - up to eight real-time PC breakpoints
 - unlimited number of real-time OPCODE breakpoints
 - Hardware execution watch-points at
 - Internal Data Memory
 - Extended Data Memory
 - Special Function Registers (SFRs)
 - Hardware watch-points activated at a certain
 - address by any write into memory
 - address by any read from memory
 - address by write into memory a required data
 - address by read from memory a required data
 - Instructions Smart Trace Buffer – configurable up to 8192 levels (optional)
 - Automatic adjustment of debug data transfer speed rate between HAD and Silicon
 - JTAG Communication interface
- **Power Management Unit**
 - Power management mode
 - Switchback feature
 - Stop mode
- **Extended Interrupt Controller**
 - 4 priority levels
 - 7 external interrupt sources (or more)
 - Up to 9 interrupt sources from peripherals
- **Four 8-bit I/O Ports**
 - Bit addressable data direction for each line
 - Read/write of single line and 8-bit group
- **Three 16-bit timer/counters**
 - Timers clocked by internal source
 - Auto reload 8/16-bit timers
 - Externally gated event counters
- **Two Full-duplex serial port**
 - Synchronous mode, fixed baud rate
 - 8-bit asynchronous mode, fixed baud rate
 - 9-bit asynchronous mode, fixed baud rate
 - 9-bit asynchronous mode, variable baud rate
- **I2C bus controller - Master**
 - 7-bit and 10-bit addressing modes
 - NORMAL, FAST, FAST+, HIGH speeds
 - Multi-master systems supported
 - Clock arbitration and synchronization
 - User defined timings on I2C lines
 - Wide range of system clock frequencies
 - Interrupt generation
- **I2C bus controller - Slave**
 - NORMAL speed 100 kB/s
 - FAST speed 400 kB/s
 - FAST+ speed 1000 kB/s
 - HIGH speed 3400 kB/s
 - Wide range of system clock frequencies
 - Interrupt generation
- **SPI – Master and Slave Serial Peripheral Interface**
 - Supports speeds up ¼ of system clock
 - Mode fault error
 - Write collision error
 - Four transfer formats supported
 - System errors detection
 - Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)

- Interrupt generation
- **Programmable Watchdog Timer**
- **16-bit Compare/Capture Unit**
 - Events capturing
 - Pulses generation
 - Digital signals generation
 - Gated timers
 - Sophisticated comparator
 - Pulse width modulation
 - Pulse width measuring
- **Fixed-Point arithmetic coprocessor**
 - Multiplication - 32bit * 32bit
 - Division - 32bit / 32bit
- **Floating-Point arithmetic coprocessor IEEE-754 standard single precision**
 - FADD, FSUB - addition, subtraction
 - FMUL, FDIV- multiplication, division
 - FSQRT- square root
 - FUCOM - compare
 - FCHS - change sign
 - FABS - absolute value
- **Floating-Point math coprocessor - IEEE-754 standard single precision real word and short integers**
 - FADD, FSUB- addition, subtraction
 - FMUL, FDIV- multiplication, division
 - FSQRT- square root
 - FUCOM- compare
 - FCHS - change sign
 - FABS - absolute value
 - FSIN, FCOS- sine, cosine
 - FTAN, FATAN- tangent, arcs tangent
- **DUSB2 – USB 2.0 device controller**
- **DMAC – Ethernet controller**
- **And more peripherals**

PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
reset	input	Global reset input
rtclk	input	RTC clock input
rtcrst	input	RTC reset input
port0i	input	Port 0 input
port1i	input	Port 1 input
port2i	input	Port 2 input
port3i	input	Port 3 input
prgdatai	input	Data bus from CODE Memory
xdmdatai	input	Data bus from EDATA Memory
xdmready	input	EDATA memory data ready
prgready	input	CODE memory data ready
idmdatai	input	Data bus from IDATA memory
sfrdatai	input	Data bus from user SFR's
int0	input	External interrupt 0
int1	input	External interrupt 1
int2	input	External interrupt 2
int3	input	External interrupt 3
int4	input	External interrupt 4
int5	input	External interrupt 5
int6	input	External interrupt 6
t0	input	Timer 0 input
t1	input	Timer 1 input
t2	input	Timer 2 input
gate0	input	Timer 0 gate input
gate1	input	Timer 1 gate input
t2ex	input	Timer 2 gate input
capture0	input	Timer 2 capture 0 line
capture1	input	Timer 2 capture 1 line
capture2	input	Timer 2 capture 2 line
capture3	input	Timer 2 capture 3 line
rxdi0	input	Serial receiver input 0
rxdi1	input	Serial receiver input 1

tdi	input	DoCD™ TAP data input
tck	input	DoCD™ TAP clock input
tms	input	DoCD™ TAP mode select input
si	input	SPI slave input
mi	input	SPI master input
scki	input	SPI clock input
ss	input	SPI slave select
scli	input	Master/Slave I2C clock line input
sdai	input	Master/Slave I2C data input
rsto	output	Reset output
port0o	output	Port 0 output
port1o	output	Port 1 output
port2o	output	Port 2 output
port3o	output	Port 3 output
prgaddr	output	CODE memory address bus
prgdatao	output	Data bus for CODE memory
prgdataz	output	Turn CODE bus into 'Z' state
prgbe	output	CODE data bus byte enable
prgrd	output	CODE memory read
prgwr	output	CODE memory write
xdmaddr	output	Address bus for EDATA memory
xmdatao	output	Data bus for EDATA memories
xmdataz	output	Turn EDATA bus into 'Z' state
xdmbe	output	EDATA data bus byte enable
xdmrd	output	Extended data memory read
xdmwr	output	Extended data memory write
xdmce	output	Extended data memory chip enable
idmaddr	output	IDATA Memory read address bus
idmwaddr	output	IDATA Memory write address bus
idmdatao	output	Data bus for IDATA memory
idmoe	output	Internal data memory output enable
idmwe	output	Internal data memory write enable
sfraddr	output	Read address bus for user SFR's
sfrwaddr	output	Write address bus for user SFR's
sfrdatao	output	Data bus for user SFR's
sfrwe	output	User SFR's read enable
sfrwr	output	User SFR's write enable
tdo	output	DoCD™ TAP data output
rtck	output	DoCD™ return clock line
debugacs	output	DoCD™ accessing data
coderun	output	CPU is executing an instruction
pmm	output	Power management mode indicator
stop	output	Stop mode indicator
rxdo0	output	Serial receiver output 0
txd0	output	Serial transmitter output 0
rxdo1	output	Serial receiver output 1
txd1	output	Serial transmitter output 1
so	output	SPI slave output
mo	output	SPI master output
scko	output	SPI clock output
scken	output	SPI clock line tri-state buffer control
sso	output	SPI slave select lines
soen	output	SPI slave output enable
sclhs	output	High speed Master I2C clock line
sclo	output	Master/Slave I2C clock output
sdao	output	Master/Slave I2C data output

CONFIGURATION

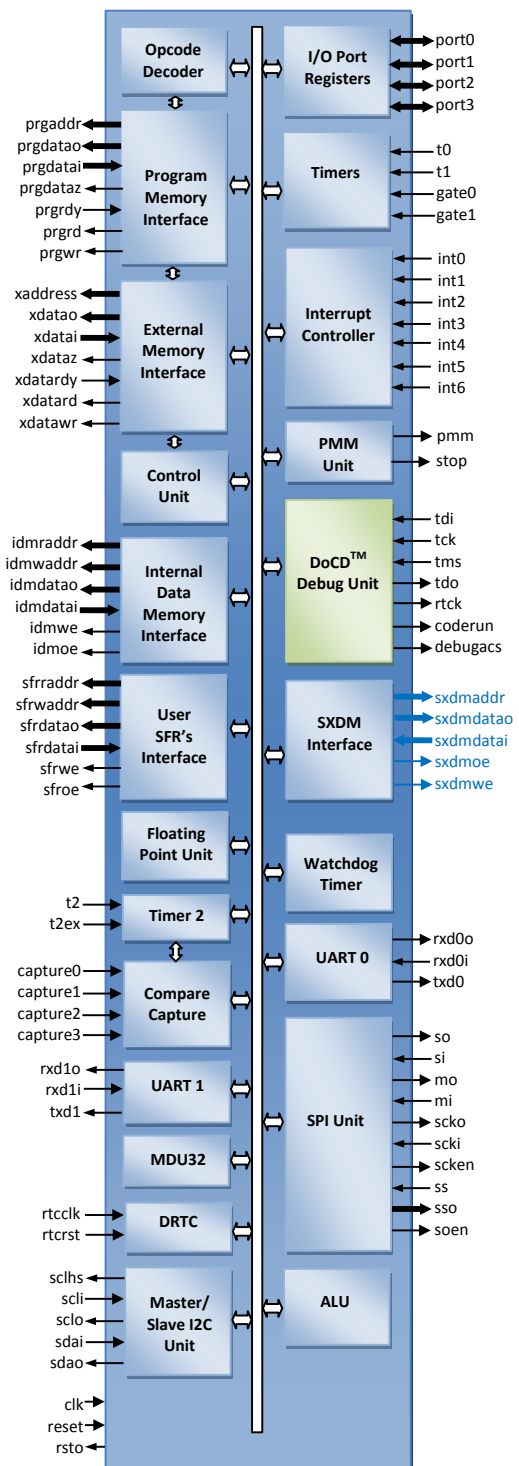
The following parameters of the DQ80251 core can be easily adjusted to requirements of a dedicated application and technology. Configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

- Program Memory size - 64kB - 8MB
- Internal Data Memory size - 1kB - 32kB
- Extended Data Memory size - 1kB - 8MB
- Program Memory Interface - synchronous
- Data Memory Interface - asynchronous

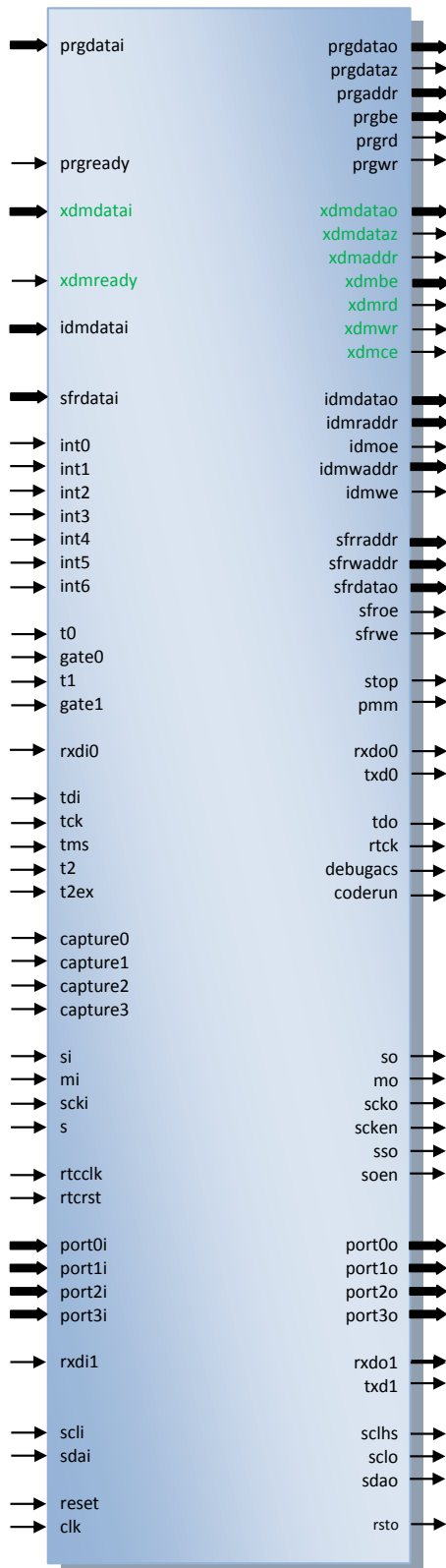
- Interrupts - subroutines location
- Power Management Mode - unused
- Stop mode - unused
- DoCD™ debug unit - enabled with selected features
- disabled

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate parameters in the package configuration file.

BLOCK DIAGRAM



SYMBOL



UNITS SUMMARY

ALU – 16/32-bit Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW, PSW1), (B)

registers and related logic, such as arithmetic unit, logic unit, multiplier and divider.

REGFILE – Contains complete set of 80251 dedicated: 8-bit {R0, R1, ..., R15} registers, 16-bit {WR0, WR2, ..., WR30} and 32-bit {DR0, DR4, ..., DR28, DR56, DR60} registers.

Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks.

Control Unit – Performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and it manages execution of all microcontroller tasks.

Program Memory Interface – Contains Program Counter (PC) and related logic. It performs instructions code fetching. Program Memory (CODE) can be also written. Program fetch cycle length can be programmed by user. This feature is called Program Memory Wait States and allows core to work with different speed program memories. It works with synchronous or asynchronous memories.

EDATA Memory Interface - Contains memory access related registers. It performs the Extended Data Memory (EDATA) addressing and data transfers. EDATA read/write cycle length can be programmed by user. EDATA covers also XDATA space from 80C51. This feature is called EDATA Memory Wait States and allows core to work with different speed memories. It is fully configurable. It works with synchronous or asynchronous memories.

Internal Data Memory Interface – Internal Data Memory interface controls access into the whole 32kB of IDATA memory. It contains 16-bit Stack Pointer (SP) register and related logic. It is fully configurable from 1 kB to 32 kB.

SFRs Interface – Special Function Registers interface controls access to the special registers. It contains standard and used defined registers and related logic. All SFR registers are bit addressable. User defined external devices, can be quickly accessed (read, written, modified), by using all direct addressing mode instructions.

Interrupt Controller – Four Levels interrupt control module is responsible for the interrupt manage system, for external and internal interrupt sources. It contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IPH, IPL) and (TCON) registers. Its upgraded version can be extended by extra user's dedicated interrupt sources. Interrupt vectors locations and spacing are fully configurable.

Timers – System timers module. Contains two 16bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 (or 4) CLK periods, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.

Ports - Block contains 8051 general purpose I/O ports. Each of ports pin can be read/write as a single bit or as an 8-bit bus P0, P1, P2, P3

Power Management Unit – contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. Switchback feature allows UARTs and interrupts to be processed in full speed mode, if enabled. It's highly desirable, when microcontroller is planned to be used in portable and power critical applications.

DoCD™ Debug Unit – a real-time hardware debugger, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal and external data, program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, REGFILE and also on SFRs. Hardware breakpoint is executed, if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins - CODERUN and DEBUGACS, indicate the state of the debugger and CPU. CODERUN is active, when CPU is executing an instruction. DEBUGACS pin is active, when any access is performed by **DoCD™** debugger. The **DoCD™** system includes JTAG interface and complete set of tools, to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off.

DRTC – provides Real Time Clock Calendar storing current time in Unix epoch format. The Unix epoch (called also POSIX time, Unix timestamp or Unix time) is the number of seconds that have elapsed since 1st January 1970 midnight UTC/GMT, not counting leap seconds (in ISO 8601: 1970-01-01T00:00:00Z). Many systems store epoch dates as a signed 32-bit integer, which might cause problems on 19th January 2038 (0x7FFFFFFF known as the Year 2038 problem). The DRTC has no such problem since its time is stored as unsigned 32-bit integer allowing correct work until 0xFFFFFFFF which is 07/Feb/2106. Additionally it can be extended to hold later future time.

Floating Point Unit – FPMU contains floating point arithmetic IEEE-754 compliant instructions (C **float**, **int**, **long int** types supported). It is used to execute single precision floating point operations such as: addition, subtraction, multiplication, division, square root, comparison absolute value of number and change of sign. Basing on specialized CORDIC algorithm, a full set of trigonometric operations is also allowed: sine, cosine, tangent, arctangent. It also has built-in integer to floating point and vice versa conversion instructions. FPU supports single precision real numbers, 16-bit and 32-bit signed integers. This unit has included standard software interface that allows easy usage and interfacing with user's C/ASM written programs.

MDU32 Multiply Divide Unit – It is a fixed point fast, 16-bit and 32-bit multiplication and division unit. It supports unsigned and 2's complement signed integer operands. The MDU32 is controlled by dedicated direct memory access module (called DMA). All arguments and result registers are automatically read and written back by internal DMA. This unit has included standard software interface, that allows easy usage and interfacing with user C/ASM written programs.

Timer 2 – Second system timer module - contains one 16-bit configurable timer: Timer 2 (TH2, TL2); capture registers (RLDH, RLDL) and Timer 2 Mode (T2MOD) register. It can work as a 16-bit timer / counter, 16-bit auto-reload timer / counter. It also supports compare capture unit if it is presented in the system. It can be used as clock source for UART0.

Compare Capture Unit – The compare/ capture/reload unit is one of the most powerful peripheral units of the core. It can be used for all kind of digital signal generation and event capturing, such as pulse generation, pulse width modulation, measurements etc.

Watchdog Timer – The watchdog timer is a 27-bit counter, which is incremented in every system clock period (CLK pin). It performs system protection against software upsets.

UART0 – Universal Asynchronous Receiver and Transmitter module is full duplex, which means, that it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning, it can commence reception of the second byte, before the previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register and reading SBUF0, reads a physically separate receive register. It works in 3 asynchronous and 1 synchronous modes. UART0 can be synchronized by Timer 1 or Timer 2 (if present in system).

UART1 – Universal Asynchronous Receiver and Transmitter module. It is full duplex (it can transmit and receive concurrently). It includes Serial Configuration register (SCON1), serial receiver and transmitter buffer (SBUF1) registers. Its receiver is double-buffered, meaning, it can commence reception of a second byte, before the previously received byte has been read from the receive register. Writing to SBUF1, loads the transmit register and reading SBUF1, reads a physically separate receive register. It works in 3 asynchronous and 1 synchronous modes. UART1 is synchronized by Timer1.

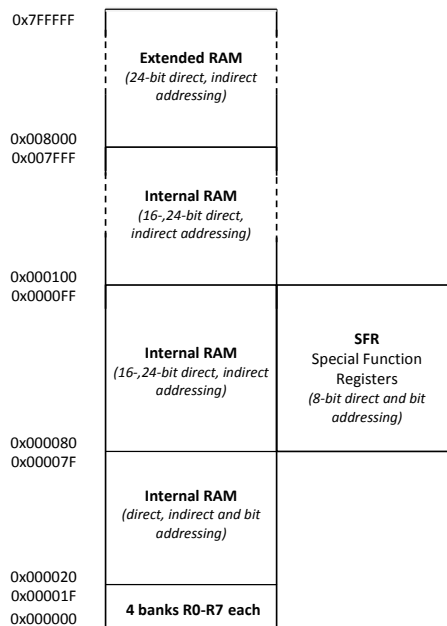
Master I2C Unit – The Master I2C Bus Controller core incorporates all features required by I2C specification. It supports both 7-bit and 10-bit addressing modes, on the I2C bus. It works as a master transmitter and receiver. It can be programmed to operate with arbitration and clock synchronization, letting it to operate in multi-master systems. Built-in timer allows operation from wide range of the input frequencies. The timer allows achieving any non-standard clock frequency. The I2C controller supports all transmission modes: Standard, Fast, Fast+ and High Speed - up to 3400kbs.

Slave I2C Unit – The Slave I2C bus controller core incorporates all features required by I2C specification. It works as a slave transmitter/receiver, depending on working mode determined by a master device. The I2C controller supports all transmission modes: Standard, Fast, Fast+ and High Speed up to 3400kbs.

SPI Unit – It's a fully configurable master/slave Serial Peripheral Interface, which allows the user to configure polarity and phase of serial clock signal SCK. It allows the microcontroller to communicate with serial peripheral devices. It is also capable of interprocessor communications in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of information on two independent serial data lines. SPI data are simultaneously transmitted and received. SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. Data rates as high as CLK/4. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of four different bit rates for the serial clock. Error-detection logic is included to support interprocessor communications. A write-collision detector indicates when an attempt is made to write data to the serial shift register while a transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers if more than one SPI devices simultaneously attempts to become bus master.

DATA MEMORY

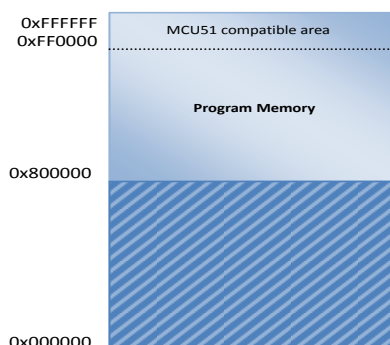
The DQ80251 has up to 32k bytes of internal data memory (IDATA) and up to 8MB of extended data memory (EDATA).



The lower internal RAM consists of four register banks, with eight registers each. The current bank is selected by a PSW register. A bit addressable segment is mapped in a range from 0x20 to 0xFF and covers part of an internal RAM and all SFR area. With the **16-, 24-bit direct or indirect** addressing mode, 0x80 to 0xFF range of the internal memory is addressed. With the **8-bit direct** addressing mode, the range from 0x80 to 0xFF SFR memory area is accessed. An extended RAM space begins just after end of an Internal RAM memory chip. For example, if the Internal RAM has 1kB size, then the Extended RAM starts at 1 kB address.

PROGRAM CODE SPACE

Program memory space begins at 0x800000 address and ends at 0xFFFFF address. It gives 8MB of code memory. The 64kB memory area, ranged from 0xFF0000 to 0xFFFFF, is intended for the MCU51 compatible code. After each reset the CPU starts execution in the program memory at 0xFF0000 location. Each interrupt has its own start address for its service routine. The interrupt vectors are also mapped, starting at 0xFF0000 location.



PERFORMANCE

The following table gives a survey about the Core area and performance in ASIC Devices:

Technology	Speed grade	Area Min [gates]	Area Full [gates]	F _{max}
0.18u	typical	14 500	23 600	150 MHz
0.13u	typical	14 200	23 000	200 MHz
0.09u	typical	13 500	21 700	300 MHz

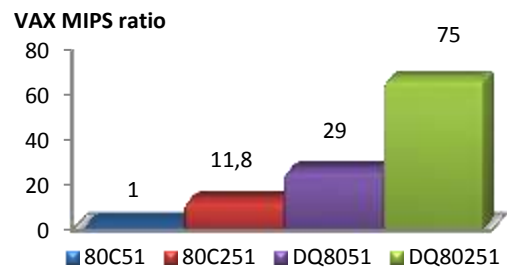
Core performance in ASIC devices – results given for working system with connected CODE and DATA memories.

The DoCD debugger increases the core size by about 2900 gates.

Dhrystone Benchmark Version 2.1 was used to measure the core performance. The following table shows the DQ80251 performance in terms of VAX MIPS per 1 MHz rating.

Device	DMIPS/MHz	Ratio
80C51	0,00941	1,00
80C251	0,11102	11,79
DQ8051	0,27297	29,01
DQ80251	0,70579	75,08

Core performance in terms of DMIPS per MHz



LICENSING

Comprehensible and clearly defined licensing methods **without royalty-per-chip fees** make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.

Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core:

- VHDL or Verilog RTL synthesizable HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM Netlist

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