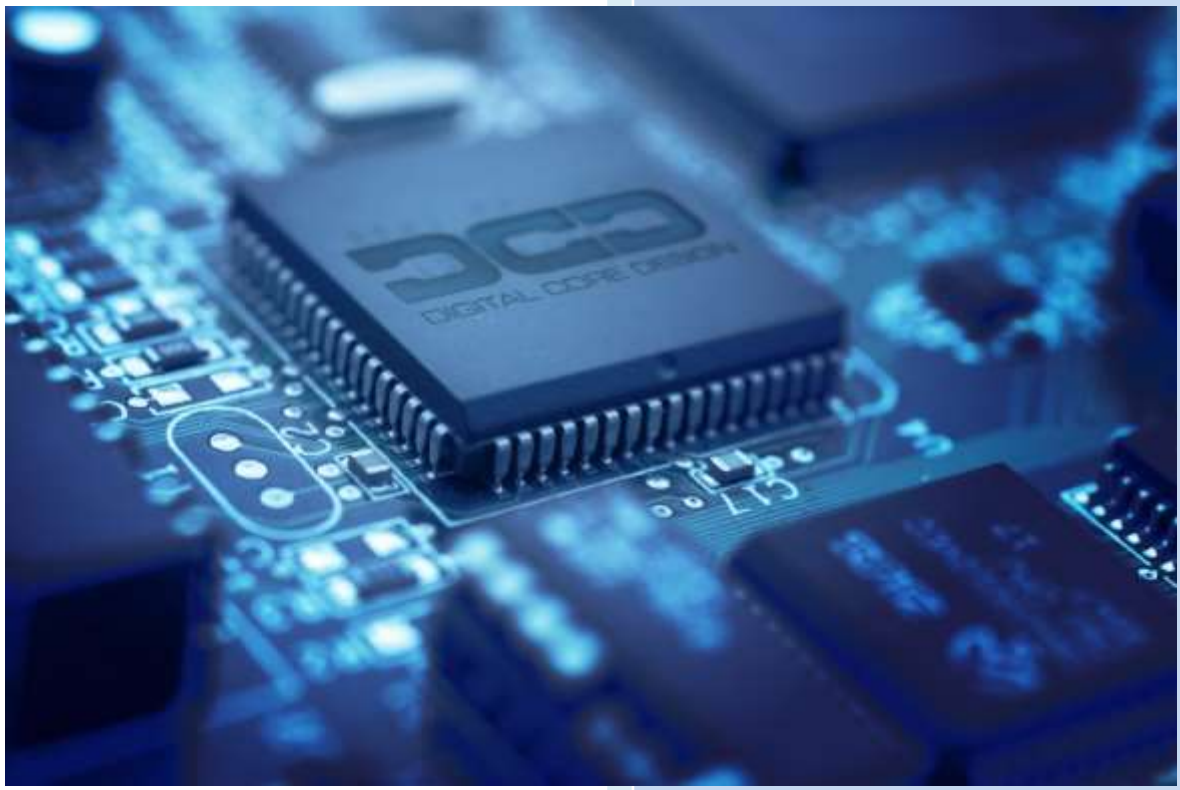
DIGITAL CORE DESIGN

2017

DP8051CPU IP Core



Pipelined High Performance 8-bit Microcontroller v. 5.02

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DP8051CPU is an **ultra-high performance, speed optimized** soft core of a single-chip 8-bit embedded controller, dedicated to operate with **fast** (typically on-chip) and **slow** (off-chip) **memories**. The core has been designed with a special concern about **performance to power consumption** ratio. This ratio is extended by an advanced power management unit - the **PMU**. The DP8051CPU soft core is 100% binary-compatible with the industry standard 8051 8-bit microcontroller. There are two configurations of the DP8051CPU: **Harvard**, where an internal data and program buses are separated and **von Neumann**, with a common program and an external data bus. The DP8051CPU has Pipelined RISC architecture **and** executes **120-300 million instructions** per second. Dhrystone 2.1 benchmark program runs from **11.46 to 15.55** times faster than the original 80C51 at the same frequency. This performance can also be exploited to a great advantage in **low power** applications, where the core can be clocked over ten times slower than the original implementation, with no performance penalty. The DP8051CPU is delivered with **fully automated test bench** and **complete set of tests**, allowing easy package validation at each stage of SoC design flow.

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates, minor and major versions changes
    - Phone & email support

CPU FEATURES

- 100% software compatible with the 8051 industry standard
- Pipelined RISC architecture enables to run 15.55 times faster than the original 80C51 at the same frequency
- Up to 14.632 VAX MIPS at 100 MHz
- 24 times faster multiplication
- 12 times faster addition
- Up to 256 bytes of internal (on-chip) Data Memory
- Up to 64K bytes of internal (on-chip) or external (off-chip) Program Memory
- Up to 16M bytes of external (off-chip) Data Memory
- User programmable Program Memory Wait States solution, for wide range of memories speed
- User programmable External Data Memory Wait States solution for wide range of memories speed
- De-multiplexed Address/Data bus to allow easy connection to memory
- Dedicated signal for Program Memory writes.
- Interface for additional Special Function Registers
- Fully synthesizable, static synchronous design with positive edge clocking and no internal tri-states
- Scan test ready

CONFIGURATION

The following parameters of the DP8051CPU core can be easily adjusted to requirements of a dedicated application and technology. The configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

• Internal Program Memory type	- synchronous - asynchronous
• Internal Program ROM Memory size	- 0 - 64kB
• Internal Program RAM Memory size	- 0 - 64kB
• Internal Program Memory fixed size	- true - false
• Interrupts	- subroutines location
• Power Management Mode	- used - unused
• Stop mode	- used - unused
• DoCD™ debug unit	- used - unused

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate constants in the package file.

DESIGN FEATURES

♦ PROGRAM MEMORY:

The DP8051CPU soft core is dedicated for operation with Internal and External Program Memory. Internal Program Memory can be implemented as:

- *ROM located in address range between 0x0000 ÷ (ROM_{size}-1)*
- *RAM located in address range between (RAM_{size}-1) ÷ 0xFFFF*

External Program Memory can be implemented as ROM or RAM located in address range between ROM_{size} ÷ RAM_{size}.

♦ INTERNAL DATA MEMORY:

The DP8051CPU can address Internal Data Memory of up to 256 bytes. The Internal Data Memory can be implemented as Single-Port synchronous RAM.

♦ EXTERNAL DATA MEMORY:

The DP8051CPU soft core can address up to 16 MB of External Data Memory. Extra DPX (*Data Pointer eXtended*) register is used for segments swapping.

♦ USER SPECIAL FUNCTION REGISTERS:

Up to 104 External (user) Special Function Registers (ESFRs) may be added to the DP8051CPU design. ESFRs are memory mapped into Direct Memory, between addresses 0x80 and 0xFF, in the same manner, as core SFRs and may occupy any address that is not occupied by a core SFR.

♦ WAIT STATES SUPPORT:

The DP8051CPU soft core is designed to be used with wide range of Program and Data memories. Slow Program and External Data memory, may assert a memory Wait signal, to hold up CPU activity.

LICENSING

Comprehensible and clearly defined licensing methods **without royalty-per-chip fees** make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.

Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.

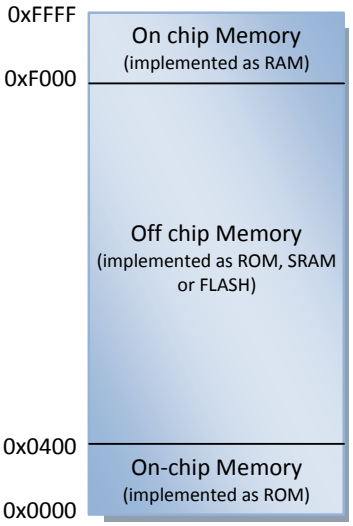
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core:

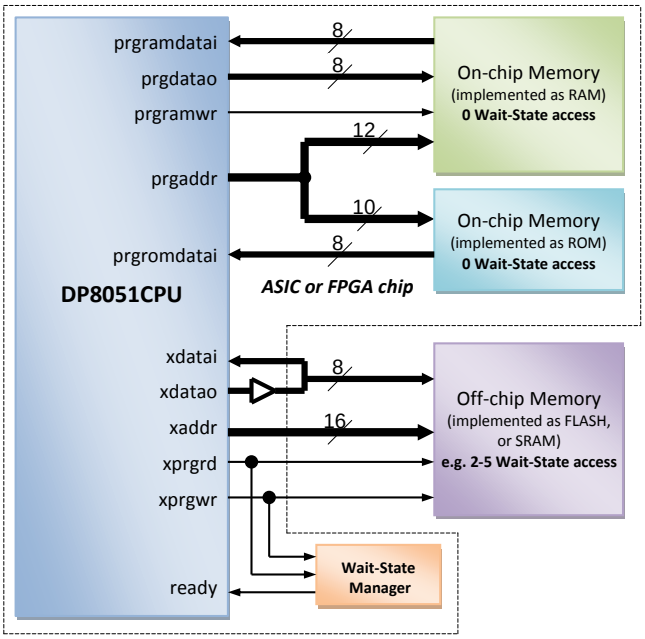
- VHDL or Verilog RTL synthesizable HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM Netlist

PROGRAM CODE SPACE IMPLEMENTATION

The following figure shows an example Program Memory space implementation in systems with the DP8051CPU Microcontroller core. The on-chip Program Memory located in an address space between 0kB and 1kB, is typically used for BOOT code with system initialization functions. This part of the code is typically implemented as ROM. The on-chip Program Memory located in an address space between 60kB and 64kB, is typically used for timing critical part of the code e.g. interrupt subroutines, arithmetic functions etc. This part of the code is typically implemented as RAM and can be loaded by the BOOT code, during initialization phase from an off-chip memory or through a RS232 interface from an external device. The program code is executed from the two spaces mentioned above without wait-states and can achieve top performance of up to 200 million instructions per second (many instructions executed in one clock cycle). The off-chip Program Memory located in an address space between 1kB and 60kB, is typically used for the main code and constants. This part of the code is usually implemented as ROM, SRAM or a FLASH device. Due to relatively long access time, the program code executed from devices mentioned above must be fetched with additional Wait-States. The number of required Wait-States depends on a memory access time and a DP8051CPU clock frequency. In most cases, the proper number of Wait-States cycles is between 2 and 5. The READY pin can be also dynamically modulated e.g. by SDRAM controller.



The figure below shows typical Program Memories connections in system with DP8051CPU Microcontroller core.



The implementation described above should be treated as an example only. All Program Memory spaces are fully configurable. For timing-critical applications the whole program code can be implemented as on-chip ROM and (or) RAM and executed without Wait-States, but for some other applications, the whole program code can be implemented as off-chip ROM or FLASH and executed with required number Wait-State cycles.

DP8051 FAMILY OVERVIEW

Main features of each DP80C51 family member have been summarized in the table below. It gives a brief member characteristic, helping you to select the most suitable IP Core for your application. You can specify your own peripheral set (including listed below and others) and requests the core modifications.

Design	Architecture speed grade	Program Memory space			Stack space size	Internal Data Memory space	External Data Memory space	External Data / Program Memory Wait States	Power Management Unit	Interface for additional SFRs	Interrupt sources	Interrupt levels	Data Pointers	Timer/Counters	UART	I\O Ports	Compare/Capture	Watchdog	Master I²C Bus Controller	Slave I²C Bus Controller	SPI	Fixed Point Coprocessor	Floating Point Coprocessor
		on-chip RAM	on-chip ROM	off-chip																			
DP8051CPU	10	64k	64k	64k	256	256	16M	✓	✓	✓	2	2	1	-	-	-	-	-	-	-	-	-	-
DP8051	10	64k	64k	64k	256	256	16M	✓	✓	✓	5	2	1	2	1	4	-	-	-	-	-	-	-
DP8051XP	10	64k	64k	64k	256	256	16M	✓	✓	✓	15	2	2	3	2	4	✓	✓	✓	✓	✓	✓	✓

DP8051 family of Pipelined High Performance Microcontroller Cores

DP80390 FAMILY OVERVIEW

Main features of each DP80390 family member have been summarized in the table below. It gives a brief member characteristic, helping you to select the most suitable IP Core for your application. You can specify your own peripheral set (including listed below and others) and requests the core modifications.

Design	Architecture speed grade	Program Memory space			Stack space size	Internal Data Memory space	External Data Memory space	External Data / Program Memory Wait States	Power Management Unit	Interface for additional SFRs	Interrupt sources	Interrupt levels	Data Pointers	Timer/Counters	UART	I\O Ports	Compare/Capture	Watchdog	Master I²C Bus Controller	Slave I²C Bus Controller	SPI	Fixed Point Coprocessor	Floating Point Coprocessor
		on-chip RAM	on-chip ROM	off-chip																			
DP80390CPU	10	64k	64k	8M	256	256	16M	✓	✓	✓	2	2	1	-	-	-	-	-	-	-	-	-	-
DP80390	10	64k	64k	8M	256	256	16M	✓	✓	✓	5	2	1	2	1	4	-	-	-	-	-	-	-
DP80390XP	10	64k	64k	8M	256	256	16M	✓	✓	✓	15	2	2	3	2	4	✓	✓	✓	✓	✓	✓	✓

DP80390 family of Pipelined High Performance Microcontroller Cores

UNITS SUMMARY

ALU – Arithmetic Logic Unit - performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic, like arithmetic unit, logic unit, multiplier and divider.

Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks.

Control Unit – It performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and it manages execution of all microcontroller tasks.

Program Memory Interface – Program Memory Interface contains Program Counter (PC) and related logic. It performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader, to load new program into ROM, RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C or DoCD™ module.

External Memory Interface - Contains memory access related registers, such as Data Page High (DPH), Data Page Low (DPL) and Data Page Pointer (DPP) registers. It performs the external Program and Data Memory addressing and data transfers. Program fetch cycle length can be programmed by the user. This feature is called Program Memory Wait States and it allows core, to work with different speed program memories.

Synchronous eXternal Data Memory (SXDM) Interface – contains XDATA memory access related logic, allowing fast access to synchronous memory devices. It performs the external Data Memory addressing and data transfers. This memory can be used, to store large variables frequently accessed by CPU, improving overall performance of application.

Internal Data Memory Interface – Interface controls access into the internal memory of size up to 256 bytes. It contains 8-bit Stack Pointer (SP) register and related logic.

User SFRs Interface – Special Function Registers interface controls access to the special registers. It contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified), by using all direct addressing mode instructions.

Interrupt Controller – Interrupt Controller module is responsible for the interrupt manage system of the external and internal interrupt sources. It contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IP) and (TCON) registers.

Power Management Unit – Power Management Unit contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. Switchback feature allows UARTs and interrupts to be pro-

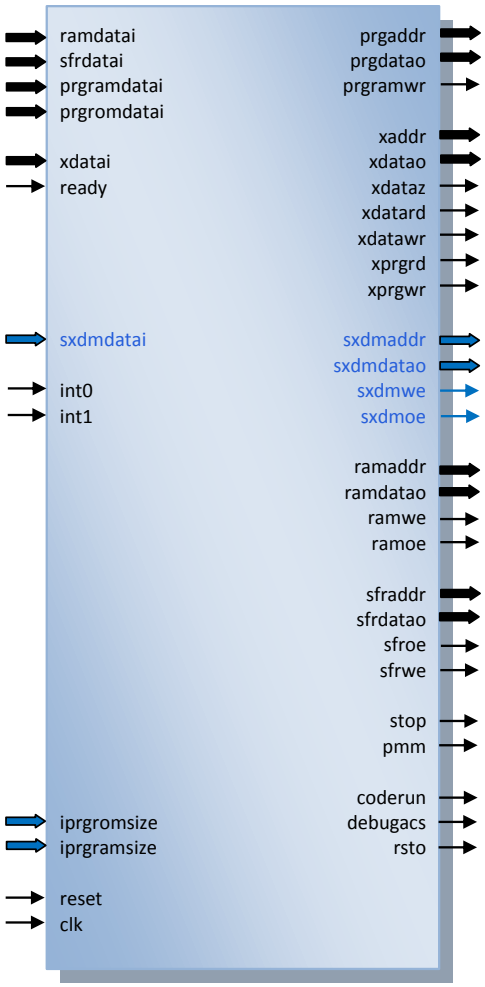
cessed in full speed mode, if enabled. It is highly desirable, when microcontroller is planned to be used in portable and power critical applications.

DoCD™ Debug Unit – it's a **real-time hardware debugger**, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** ensures **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware watchpoints can be set and controlled on internal and external data memories and also on SFRs. Hardware watchpoints are executed, if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins: CODERUN and DEBUGACS, indicate the state of the debugger and CPU. CODERUN is active, when CPU is executing an instruction. DEBUGACS pin is active, when any access is performed by **DoCD™** debugger. The **DoCD™** system includes **TTAG** or **JTAG interface** and complete set of tools, to communicate and work with core in real time debugging. It is built, as a scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off.

PERIPHERALS

- DoCD™ debug unit
  - *Processor execution control*
    - *Run, Halt*
    - *Step into instruction*
    - *Skip instruction*
  - *Read-write all processor contents*
    - *Program Counter (PC)*
    - *Program Memory*
    - *Internal (direct) Data Memory*
    - *Special Function Registers (SFRs)*
    - *External Data Memory*
  - *Code execution breakpoints*
    - *up to eight real-time PC breakpoints*
    - *unlimited number of real-time OPCODE breakpoints*
  - *Hardware execution watch-points at*
    - *Internal (direct) Data Memory*
    - *Special Function Registers (SFRs)*
    - *External Data Memory*
  - *Hardware watch-points activated at certain:*
    - *address by any write into memory*
    - *address by any read from memory*
    - *address by required data write into memory*
    - *address by required data read from memory*
  - *Instructions Smart Trace Buffer – configurable up to 8192 levels (optional)*
  - *Automatic adjustment of debug data transfer speed rate between HAD and Silicon*
  - *TTAG or JTAG Communication interface*
- Power Management Unit
  - *Power management mode*
  - *Switchback feature*
  - *Stop mode*
- Interrupt Controller
  - *2 priority levels*
  - *2 external interrupt sources*

SYMBOL

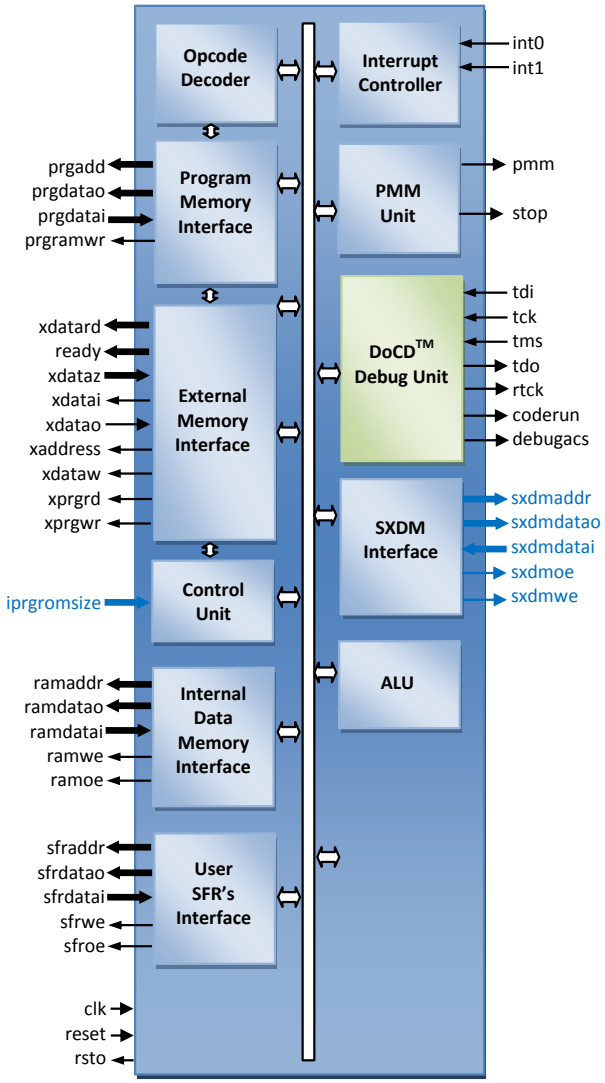


PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
reset	input	Global reset
port0i	input	Port 0 input
port1i	input	Port 1 input
port2i	input	Port 2 input
port3i	input	Port 3 input
iprgramsize	input	Size of on-chip RAM CODE
iprgromsize	input	Size of on-chip ROM CODE
prgramdata	input	Data bus from int. RAM prog. memory
prgromdata	input	Data bus from int. ROM prog. memory
sxdmdatai	input	Data bus from sync external data memory (SXDM)
xdatai	input	Data bus from external memories
ready	input	External memory data ready
ramdatai	input	Data bus from internal data memory
sfrdatai	input	Data bus from user SFR's
int0	input	External interrupt 0
int1	input	External interrupt 1
tdi	input	DoCD™ TAP data input
tck	input	DoCD™ TAP clock input
tms	input	DoCD™ TAP mode select input
rsto	output	Reset output
port0o	output	Port 0 output
port1o	output	Port 1 output
port2o	output	Port 2 output
port3o	output	Port 3 output
prgaddr	output	Internal program memory address bus
prgdatao	output	Data bus for internal program memory

prgramwr	output	Internal program memory write
sxdmaddr	output	Sync XDATA memory address bus (SXDM)
sxdmdatao	output	Data bus for Sync XDATA memory (SXDM)
sxdmoe	output	Sync XDATA memory read (SXDM)
sxdmwe	output	Sync XDATA memory write (SXDM)
xaddr	output	Address bus for external memories
xdatao	output	Data bus for external memories
xdataz	output	Turn xdata bus into 'Z' state
xprgrd	output	External program memory read
xprgwr	output	External program memory write
xdatard	output	External data memory read
xdatawr	output	External data memory write
ramaddr	output	Internal Data Memory address bus
ramdatao	output	Data bus for internal data memory
ramoe	output	Internal data memory output enable
ramwe	output	Internal data memory write enable
sfraddr	output	Address bus for user SFR's
sfrdatao	output	Data bus for user SFR's
sfroe	output	User SFR's read enable
sfrwe	output	User SFR's write enable
tdo	output	DoCD™ TAP data output
rtck	output	DoCD™ return clock line
debugacs	output	DoCD™ accessing data
coderun	output	CPU is executing an instruction
pmm	output	Power management mode indicator
stop	output	Stop mode indicator

BLOCK DIAGRAM



PERFORMANCE

The following table gives a survey about the Core area and performance in Programmable Logic Devices after Place & Route (all CPU features and peripherals have been included):

Technology / optimization	Speed grade	Area [gates]	F_{max}
0.25u area	typical	6 050	100 MHz
0.25u speed	typical	7 600	250 MHz
0.18u area	typical	5 730	100 MHz
0.18u speed	typical	6 900	300 MHz

Core performance in ASIC devices – results given for working system with connected IDATA, CODE and XDATA memories. DoCD debugger increases core size about 2100 gates.

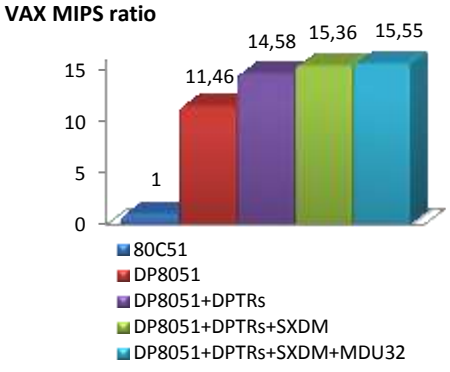
For the user, the most important factor is an application speed improvement. The most commonly used arithmetic functions and their improvements are shown in the table below. An improvement was computed as {80C51 clock periods} divided by {DP8051CPU clock periods} required to execute an identical function. More details are available in the core documentation.

Function	Improvement
8-bit addition (*immediate data*)	**9,00**
8-bit addition (*direct addressing*)	**9,00**
8-bit addition (*indirect addressing*)	**9,00**
8-bit addition (*register addressing*)	**12,00**
8-bit subtraction (*immediate data*)	**9,00**
8-bit subtraction (*direct addressing*)	**9,00**
8-bit subtraction (*indirect addressing*)	**9,00**
8-bit subtraction (*register addressing*)	**12,00**
8-bit multiplication	**16,00**
8-bit division	**9,60**
16-bit addition	**12,00**
16-bit subtraction	**12,00**
16-bit multiplication	**13,60**
32-bit addition	**12,00**
32-bit subtraction	**12,00**
32-bit multiplication	**12,60**
Average speed improvement:	**11,12**

Dhrystone Benchmark Version 2.1 was used to measure the Core performance. The following table shows the DP8051 performance in terms of VAX MIPS per 1 MHz rating.

Device	DMIPS/MHz	Ratio
80C51	0,00941	1,00
DP8051	0,10787	11,46
DP8051+DPTRs	0,13722	14,58
DP8051+DPTRs+SXDM	0,14457	15,36
DP8051+DPTRs+SXDM+MDU32	0,14632	15,55

Core performance in terms of DMIPS per MHz



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