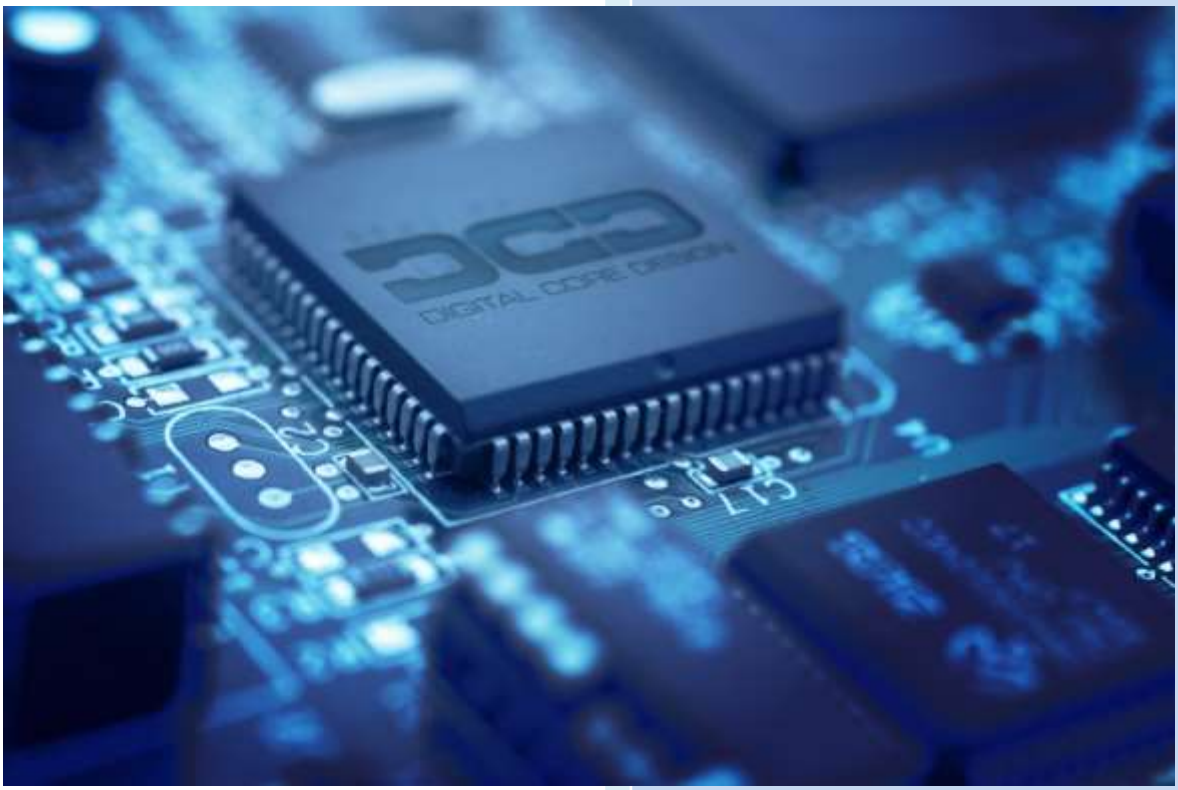
DIGITAL CORE DESIGN

2017

DQ8051XP IP Core



Revolutionary Quad-Pipelined Ultra High Performance 8-bit Microcontroller v. 6.00

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DQ8051XP is an **ultra-high performance, speed optimized** soft core of a single-chip 8-bit embedded controller, designed to operate with fast (typically on-chip) and slow (off-chip) memories. The core has been designed with a special concern about performance to power consumption ratio. This ratio is extended by an **Advanced Power Management Unit –** the **PMU**. The DQ8051XP soft core is 100% binary-compatible with the industry standard 8051 8-bit microcontroller. The DQ8051 has a built-in configurable DoCD-JTAG on-chip debugger, supporting Keil µVision development platform and a standalone DoCD debug software. **Dhrystone 2.1 benchmark program runs from 19.69 to 26.62 times faster than the original 80C51 at the same frequency**. This performance can be also exploited to a great advantage in low power applications, where the core can be clocked over ten times more slowly than the original implementation, with no performance penalty. The DQ8051XP is fully customizable - it is delivered in the exact configuration to meet your requirements. The DQ8051XP is delivered with fully automated test bench and complete set of tests, allowing easy package validation at each stage of SoC design flow.

CPU FEATURES

- 100% software compatible with the 8051 industry standard
- Quad-Pipelined architecture enables to run 26.62 times faster than the original 80C51, at the same frequency
- Up to 25.053 VAX MIPS at 100 MHz
- 24 times faster multiplication
- 12 times faster addition
- 2 Data Pointers (DPTR) for faster memory blocks copying
  - *Advanced INC & DEC modes*
  - *Auto-switch of current DPTR*
- Up to 256 bytes of internal (on-chip) Data Memory - IDM
- Up to 64K bytes of Program Memory
- Up to 16M bytes of external (off-chip) Data Memory - XDM
  - *Synchronous interface for up to 64K bytes of (on-chip) fast external Data Memory - (SXDM)*
- User programmable Program Memory Wait States solution for wide range of memories speed
- User programmable External Data Memory Wait States solution for wide range of memories speed
- De-multiplexed Address/Data bus to allow easy connection to memory
- Interface for additional Special Function Registers
- Fully synthesizable, static synchronous design with no internal tri-states
- Scan test ready

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates, minor and major versions changes
    - Phone & email support

PERIPHERALS

- DoCD™ debug unit
  - *Processor execution control*
    - *Run, Halt*
    - *Step into instruction*
    - *Skip instruction*
  - *Read-write all processor contents*
    - *Program Counter (PC)*
    - *Program Memory*
    - *Internal (direct) Data Memory*
    - *Special Function Registers (SFRs)*
    - *External Data Memory*
  - *Code execution breakpoints*
    - *up to eight real-time PC breakpoints*
    - *unlimited number of real-time OPCODE breakpoints*
  - *Hardware execution watch-points at*
    - *Internal (direct) Data Memory*
    - *Special Function Registers (SFRs)*
    - *External Data Memory*
  - *Hardware watch-points activated at a certain*
    - *address by any write into memory*
    - *address by any read from memory*
    - *address by write into memory a required data*
    - *address by read from memory a required data*
  - *Instructions Smart Trace Buffer – configurable up to 8192 levels (optional)*
  - *Automatic adjustment of debug data transfer speed rate between HAD and Silicon*
  - *JTAG Communication interface*
- Power Management Unit
  - *Power management mode*
  - *Switchback feature*
  - *Stop mode*
- Extended Interrupt Controller
  - *2 priority levels*
  - *Up to 7 external interrupt sources*
  - *Up to 8 interrupt sources from peripherals*
- Four 8-bit I/O Ports
  - *Bit addressable data direction for each line*
  - *Read/write of single line and 8-bit group*
- Three 16-bit timer/counters
  - *Timers clocked by internal source*
  - *Auto reload 8/16-bit timers*

- *Externally gated event counters*
- Two full-duplex serial ports
  - *Synchronous mode, fixed baud rate*
  - *8-bit asynchronous mode, fixed baud rate*
  - *9-bit asynchronous mode, fixed baud rate*
  - *9-bit asynchronous mode, variable baud rate*
- I2C bus controller - Master
  - *7-bit and 10-bit addressing modes*
  - *NORMAL, FAST, FAST+, HIGH speeds*
  - *Multi-master systems supported*
  - *Clock arbitration and synchronization*
  - *User defined timings on I2C lines*
  - *Wide range of system clock frequencies*
  - *Interrupt generation*
- I2C bus controller - Slave
  - *NORMAL speed 100 kB/s*
  - *FAST speed 400 kB/s*
  - *FAST+ speed 1000 kB/s*
  - *HIGH speed 3400 kB/s*
  - *Wide range of system clock frequencies*
  - *User defined data setup time on I2C lines*
  - *Interrupt generation*
- SPI – Master and Slave Serial Peripheral Interface
  - *Supports speeds up ¼ of system clock*
    - *Mode fault error*
    - *Write collision error*
  - *Four transfer formats supported*
  - *System errors detection*
  - *Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)*
  - *Interrupt generation*
- Programmable Watchdog Timer
- 16-bit Compare/Capture Unit
  - *Events capturing*
  - *Pulses generation*
  - *Digital signals generation*
  - *Gated timers*
  - *Sophisticated comparator*
  - *Pulse width modulation*
  - *Pulse width measuring*
- Fixed-Point arithmetic coprocessor
  - *Multiplication - 16bit * 16bit*
  - *Multiplication - 32bit * 32bit*
  - *Division - 32bit / 32bit*
  - *Division - 16bit / 16bit*
- Floating-Point arithmetic coprocessor IEEE-754 standard single precision
  - *FADD, FSUB - addition, subtraction*
  - *FMUL, FDIV- multiplication, division*
  - *FSQRT- square root*
  - *FUCOM - compare*
  - *FCHS - change sign*
  - *FABS - absolute value*
- Floating-Point math coprocessor - IEEE-754 standard single precision real, word and short integers
  - *FADD, FSUB- addition, subtraction*
  - *FMUL, FDIV- multiplication, division*
  - *FSQRT- square root*
  - *FUCOM- compare*
  - *FCHS - change sign*
  - *FABS - absolute value*
  - *FSIN, FCOS- sine, cosine*
  - *FTAN, FATAN- tangent, arcs tangent*
- And more peripherals

DESIGN FEATURES

♦ PROGRAM MEMORY:

The DQ8051XP soft core is dedicated for operation with Internal or External Program Memory. Program Memory can be implemented as ROM, RAM or FLASH.

♦ INTERNAL DATA MEMORY:

The DQ8051XP can address Internal Data Memory of up to 256 bytes The Internal Data Memory can be implemented as synchronous RAM.

♦ EXTERNAL DATA MEMORY:

The DQ8051XP soft core can address up to 16MB of External Data Memory. Extra DPX (*Data Pointer eXtended*) register is used for segments swapping.

♦ SYNCHRONOUS XDM:

The DQ8051XP soft core can address up to 64kB of fast on-chip Synchronous External Data Memory. All reads and writes are executed in one clock cycle.

♦ USER SPECIAL FUNCTION REGISTERS:

Up to 60 External (user) Special Function Registers (ESFRs) may be added to the DQ8051XP design. ESFRs are memory mapped into Direct Memory between addresses 0x80 and 0xFF, in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR.

♦ WAIT STATES SUPPORT:

The DQ8051XP soft core is dedicated for operation with wide range of Program and Data memories. Slow Program and External Data memory may assert a memory Wait signal to hold up CPU activity.

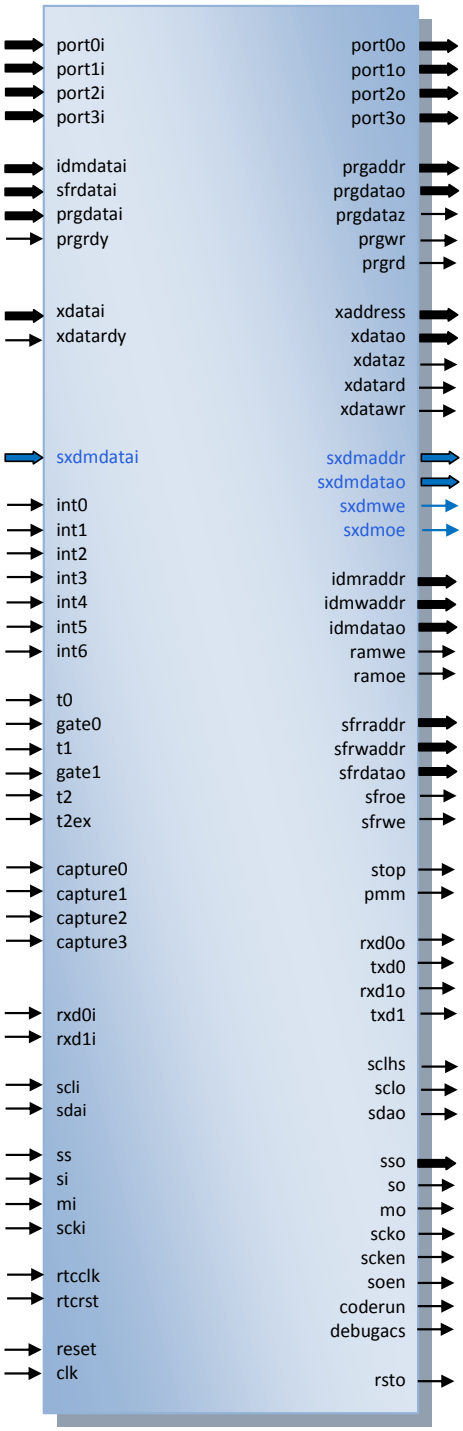
CONFIGURATION

The following parameters of the DQ8051XP core can be easily adjusted to requirements of a dedicated application and technology. The configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

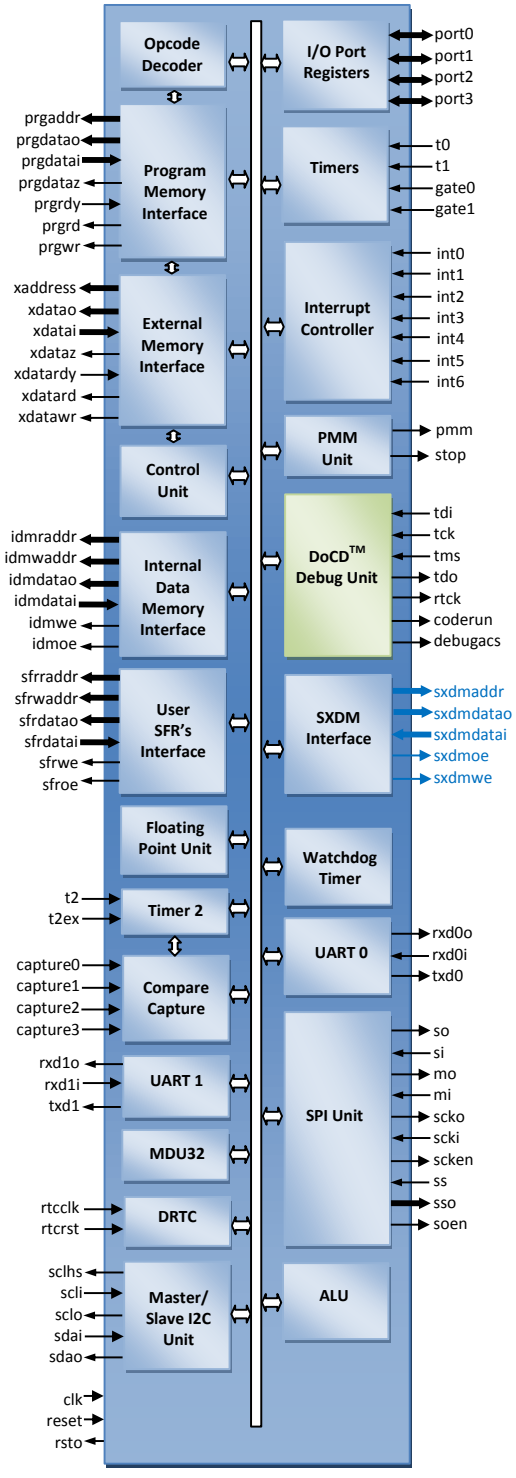
- Second Data Pointer (DPTR1) - used / - unused
- DPTR0 decrement - used / - unused
- DPTR1 decrement - used / - unused
- Data Pointers auto-switch - used / - unused
- Data Pointers auto-update - used / - unused
- Interrupts - subroutines location
- Timing access protection - used / - unused
- Power Management Mode - used / - unused
- Stop mode - used / - unused
- Peripherals - used / - unused
- Synchronous XDM - size
- DoCD™ debug unit - used / - unused

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate constants in the package file.

SYMBOL



BLOCK DIAGRAM



PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
reset	input	Global reset
rtcclk	input	RTC clock input
rtcrst	input	RTC reset input
port0i	input	Port 0 input
port1i	input	Port 1 input
port2i	input	Port 2 input
port3i	input	Port 3 input
prgdatai	input	Data bus from program memory
prgrdy	input	Program memory ready
xdmdatai	input	Data bus from synchronous external data memory (SXDM)
xdatai	input	Data bus from external memories
xdatardy	input	External data memory ready
idmdatai	input	Data bus from internal data memory
sfrdatai	input	Data bus from user SFR's
int0	input	External interrupt 0
int1	input	External interrupt 1
int2	input	External interrupt 2
int3	input	External interrupt 3
int4	input	External interrupt 4
int5	input	External interrupt 5
int6	input	External interrupt 6
t0	input	Timer 0 input
t1	input	Timer 1 input
t2	input	Timer 2 input
gate0	input	Timer 0 gate input
gate1	input	Timer 1 gate input
t2ex	input	Timer 2 gate input
capture0	input	Timer 2 capture 0 line
capture1	input	Timer 2 capture 1 line
capture2	input	Timer 2 capture 2 line
capture3	input	Timer 2 capture 3 line
rxdi0	input	Serial receiver input 0
rxdi1	input	Serial receiver input 1
scli	input	Master/Slave I2C clock line input
sdai	input	Master/Slave I2C data input
ss	input	SPI slave select
si	input	SPI slave input
mi	input	SPI master input
scki	input	SPI clock input
tdi	input	DoCD™ TAP data input
tck	input	DoCD™ TAP clock input
tms	input	DoCD™ TAP mode select input
rsto	output	Reset output
port0o	output	Port 0 output
port1o	output	Port 1 output
port2o	output	Port 2 output
port3o	output	Port 3 output
prgaddr	output	Internal program memory address bus
prgdatao	output	Data bus for internal program memory
prgdataz	output	Turn prgdata bus into 'Z' state
prgwr	output	Program memory write
prgrd	output	Program memory read
sxdmaddr	output	Synchronous XDATA memory address bus
xdmdatao	output	Data bus for Synchronous XDATA memory
sxdmoe	output	Synchronous XDATA memory read
sxdmwe	output	Synchronous XDATA memory write
xaddress	output	Address bus for external data memory
xdatao	output	Data bus for external data memory
xdataz	output	Turn xdata bus into 'Z' state
xdatard	output	External data memory read
xdatawr	output	External data memory write
idmraddr	output	IDM read address bus
idmwaddr	output	IDM write address bus
idmdatao	output	Data bus for internal data memory
idmoe	output	Internal data memory output enable
idmwe	output	Internal data memory write enable
sfrraddr	output	Read address bus for user SFR's
sfrwaddr	output	Write address bus for user SFR's
sfrdatao	output	Data bus for user SFR's
sfroe	output	User SFR's read enable
sfrwe	output	User SFR's write enable
tdo	output	DoCD™ TAP data output
rtck	output	DoCD™ return clock line
debugacs	output	DoCD™ accessing data
coderun	output	CPU is executing an instruction
pmm	output	Power management mode indicator
stop	output	Stop mode indicator
rxd0o	output	Serial receiver output 0
rxd1o	output	Serial receiver output 1
txd0	output	Serial transmitter output 0
txd1	output	Serial transmitter output 1
sclo	output	Master/Slave I2C clock output
sclhs	output	High speed Master I2C clock line
sdao	output	Master/Slave I2C data output
sso	output	SPI slave select lines
so	output	SPI slave output
mo	output	SPI master output
scko	output	SPI clock output
scken	output	SPI clock line tri-state buffer control
soen	output	SPI slave output enable

UNITS SUMMARY

ALU – Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic, like arithmetic unit, logic unit, multiplier and divider.

Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks.

Control Unit – It performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and it manages execution of all microcontroller tasks.

Program Memory Interface – Program Memory Interface contains Program Counter (PC) and related logic. It performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader, to load new program into ROM, RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C or DoCD™ module.

External Data Memory Interface - It contains memory access related registers, such as Data Pointer High (DPH), Data Pointer Low (DPL), Data Page Pointer (DPP), MOVX @Ri address register (MXAX) and STRETCH registers. It performs the memory addressing and data transfers. It also allows applications software to access up to 16MB of external data memory. The DPP register is used for segments swapping. STRETCH register allows flexible timing management, while accessing different speed system devices, by programming XDATAWR and XDATARD pulse width between 1 and 8 clock periods.

Synchronous eXternal Data Memory (SXDM) Interface – contains XDATA memory access related logic, allowing fast access to synchronous memory devices. It performs the external Data Memory addressing and data transfers. This memory can be used to store large variables, frequently accessed by CPU, improving overall performance of application.

Internal Data Memory Interface – Interface controls access to the internal memory of size up to 256 bytes. It contains 8-bit Stack Pointer (SP) register and related logic.

User SFRs Interface – Special Function Registers interface controls access to the special registers. It contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified), by using all direct addressing mode instructions.

Interrupt Controller – Interrupt control module is responsible for the interrupt manage system for the external and internal interrupt sources. It contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IP), Extended Interrupt Enable (EIE), Extended Interrupt priority (EIP) and (TCON) registers.

I/O Ports – Block contains 8051's general purpose I/O ports. Each of port's pin can be read/write as a single bit or as an 8-bit bus called P0, P1, P2, and P3.

Power Management Unit – Power Management Unit contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. Switchback feature allows UARTs and interrupts to be processed in full speed mode, if enabled. It's highly desirable, when microcontroller is planned to be used in portable and power critical applications.

DoCD™ Debug Unit – it's a **real-time hardware debugger**, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** ensures **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware watchpoints can be set and controlled on internal and external data memories and also on SFRs. Hardware watchpoints are executed, if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins: CODERUN and DEBUGACS, indicate the state of the debugger and CPU. CODERUN is active, when CPU is executing an instruction. DEBUGACS pin is active, when any access is performed by **DoCD™** debugger. The **DoCD™** system includes **JTAG interface** and complete set of tools, to communicate and work with core in real time debugging. It is built, as a scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off.

DRTC – provides Real Time Clock Calendar storing current time in Unix epoch format. The Unix epoch (called also POSIX time, Unix timestamp or Unix time) is the number of seconds that have elapsed since 1st January 1970 midnight UTC/GMT, not counting leap seconds (in ISO 8601: 1970-01-01T00:00:00Z). Many systems store epoch dates as a signed 32-bit integer, which might cause problems on 19th January 2038 (0x7FFFFFFF known as the Year 2038 problem). The DRTC has no such problem since its time is stored as unsigned 32-bit integer allowing correct work until 0xFFFFFFFF which is 07/Feb/2106. Additionally it can be extended to hold later future time.

Floating Point Unit – FPMU contains floating point arithmetic IEEE-754 compliant instructions (C **float, int, long int** types supported). It is used to execute single precision floating point operations such as: addition, subtraction, multiplication, division, square root, comparison absolute value of number and change of sign. Basing on specialized CORDIC algorithm, a full set of trigonometric operations is also allowed: sine, cosine, tangent, arctangent. It also has built-in integer to floating point and vice versa conversion instructions. FPU supports single precision real numbers, 16-bit and 32-bit signed integers. This unit has included standard software interface that allows easy usage and interfacing with user's C/ASM written programs.

MDU32 Multiply Divide Unit – It is a fixed point fast, 16-bit and 32-bit multiplication and division unit. It supports unsigned and 2,s complement signed integer operands. The MDU32 is controlled by dedicated direct memory access module (called DMA). All arguments and result registers are automatically read and written back by internal DMA. This unit has included standard software interface, that allows easy usage and interfacing with user C/ASM written programs. **This module is a modern replacement for older MDU.**

Timers – System timers module. Contains two 16bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 (or 4) CLK periods, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.

Timer 2 – Second system timer module - contains one 16-bit configurable timer: Timer 2 (TH2, TL2); capture registers (RLDH, RLDL) and Timer 2 Mode (T2MOD) register. It can work as a 16-bit timer / counter, 16-bit auto-reload timer / counter. It also supports compare capture unit if it is presented in the system. It can be used as clock source for UART0.

Compare Capture Unit – A compare/capture/reload unit is one of the most powerful peripheral units of the core. It can be used for all kind of digital signal generation and event capturing, such as pulse generation, pulse width modulation, measurements etc.

Watchdog Timer – The watchdog timer is a 27-bit counter, which is incremented in every system clock period (CLK pin). It performs system protection against software upsets.

UART0 – Universal Asynchronous Receiver and Transmitter module is full duplex, which means, that it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning, it can commence reception of the second byte, before the previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register and reading SBUF0, reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART0 can be synchronized by Timer 1 or Timer 2 (if present in system).

UART1 – Universal Asynchronous Receiver and Transmitter module. It is full duplex, which means, that it can transmit and receive concurrently. Includes Serial Configuration register (SCON1), serial receiver and transmitter buffer (SBUF1) registers. Its receiver is double-buffered, meaning, it can commence reception of a second byte, before the previously received byte has been read from the receive register. Writing to SBUF1, loads the transmit register and reading SBUF1, reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART1 is synchronized by Timer1.

Master I2C Unit – The Master I2C Bus Controller core incorporates all features required by I2C specification. Supports both 7-bit and 10-bit addressing modes, on the I2C bus. It works as a master transmitter and receiver. It can be programmed to operate with arbitration and clock synchronization, letting it to operate in multi-master systems. Built-in timer allows operation from wide range of input frequencies. The timer allows achieving any non-standard clock frequency. The I2C controller supports all transmission modes: Standard, Fast, Fast+ and High Speed - up to 3400kbs.

Slave I2C Unit – The Slave I2C bus controller core incorporates all features required by I2C specification. It works as a slave transmitter/receiver, depending on working mode determined by a master device. The I2C controller supports all transmission modes: Standard, Fast, Fast+ and High Speed up to 3400kbs.

SPI Unit – It's a fully configurable master/slave Serial Peripheral Interface, which allows user to configure polarity and phase of serial clock signal SCK. It allows the microcontroller to communicate with serial peripheral devices. It is also capable of interprocessor communications in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. SPI data are simultaneously transmitted and received. SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. Data rates as high as CLK/4. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of four different bit rates for the serial clock. Error-detection logic is included to support interprocessor communications. A write-collision detector indicates when an attempt is made to write data to the serial shift register while a transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers if more than one SPI devices simultaneously attempts to become bus master.

LICENSING

Comprehensible and clearly defined licensing methods **without royalty-per-chip fees** make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.

Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core:

- VHDL or Verilog RTL synthesizable HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM Netlist

DQ8051 FAMILY OVERVIEW

The main features of each DQ8051 family member have been summarized in the table below. It gives a brief member characteristic, helping you to select the most suitable IP Core for your application. You can specify your own peripheral set (including listed below and others) and requests the core modifications.

Design	Architecture speed grade	Program Memory space			Stack space size	Internal Data Memory space	External Data Memory space	External Data / Program Memory Wait States	Power Management Unit	Interface for additional SFRs	Interrupt sources	Interrupt levels	Data Pointers	Timer/Counters	UART	I\O Ports	Compare/Capture	Watchdog	Master I^2C Bus Controller	Slave I^2C Bus Controller	SPI	Fixed Point Coprocessor	Floating Point Coprocessor
		on-chip RAM	on-chip ROM	off-chip																			
DQ8051CPU	25.1	64k	64k	64k	256	256	16M	✓	✓	✓	2	2	2	-	-	-	-	-	-	-	-	-	-
DQ8051	25.1	64k	64k	64k	256	256	16M	✓	✓	✓	5	2	2	2	1	4	-	-	-	-	-	-	-
DQ8051XP	26.6	64k	64k	64k	256	256	16M	✓	✓	✓	15	2	2	3	2	4	✓	✓	✓	✓	✓	✓	✓

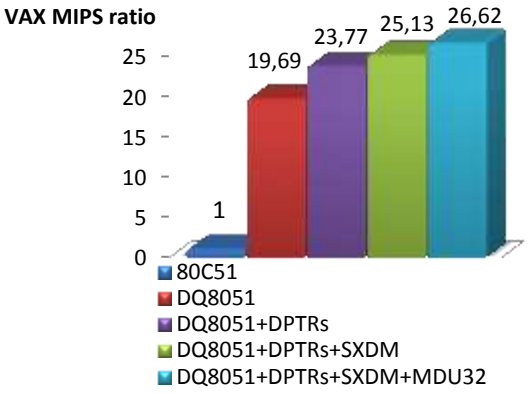
DQ8051 family of Pipelined High Performance Microcontroller Cores

PERFORMANCE

One of the most important performance parameters is a real application speed improvement, comparing to the well-known 80C51 architecture. The Dhrystone Benchmark Version 2.1 was used to measure the 80C51 and the DQ8051XP core performance. The following table gives a survey about the DQ8051XP performance, in terms of Dhrystone VAX MIPS per 1 MHz and its improvement, comparing to the 80C51.

Device	DMIPS/MHz	Ratio
80C51	0,00941	1,00
DQ8051	0,18527	19,69
DQ8051+DPTRs	0,22369	23,77
DQ8051+DPTRs+SXDM	0,23650	25,13
DQ8051+DPTRs+SXDM+MDU32	0,25053	26,62

Core performance in terms of DMIPS per MHz



The following table gives a survey about the DQ8051XP core area in INTEL FPGA Programmable Logic Devices after Place & Route (CPU features and peripherals included):

Device	Speed	Min area	F_{max}
CYCLONE-II	-6	5350 LC	40 MHz
CYCLONE-III	-6	5350 LC	50 MHz
CYCLONE-IV GX	-6	5350 LC	50 MHz
STRATIX-II	-3	3550 LUT	70 MHz
STRATIX-III	-2	3550 LUT	100 MHz
STRATIX-IV	-1	3550 LUT	90 MHz
STRATIX-V	-2	3550 LUT	90 MHz

DQ8051 core area and performance in INTEL FPGA® devices.
Results given for working system with two DPTRs and connected 256B IDM, 8kB CODE and 2kB SXDM memories.

CONTACT

Digital Core Design Headquarters:

Wroclawska 94, 41-902 Bytom, POLAND

e-mail: info@dcd.pl
tel.: 0048 32 282 82 66
fax: 0048 32 282 74 37

Distributors:

Please check: http://dcd.pl/sales