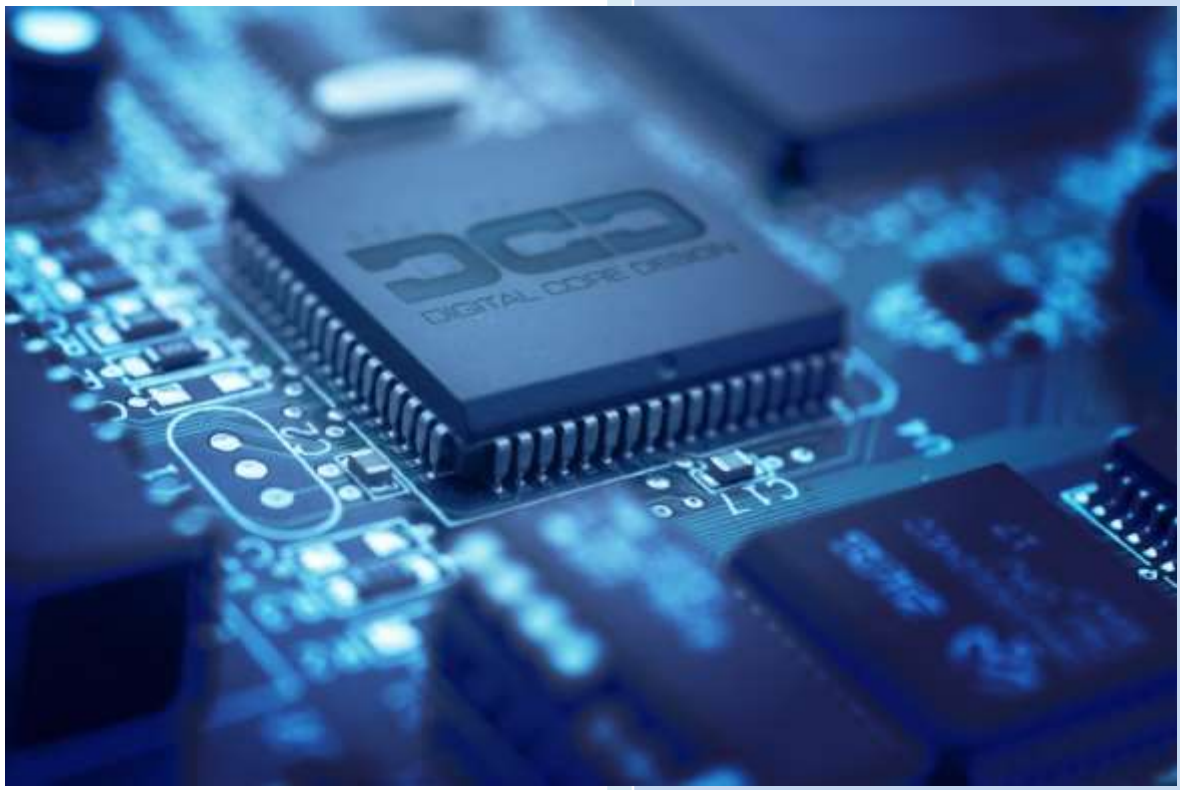
DIGITAL CORE DESIGN

2017

DI2CSB IP Core



I2C Bus Interface Slave - Base version v. 3.00

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The I^2C is a two-wire, bi-directional serial bus, which provides simple and efficient method of data transmission over a short distance, between many devices. The DI2CSB provides an interface between passive target devices e.g. memory, LCD display, pressure sensors etc. and an I2C bus. It can work as a slave receiver or transmitter, depending on a working mode, determined by the master device. A very simple interface, composed with the read, write and data signals, allows easy connection with target devices. The core doesn't require programming and is ready to work after power-up/reset. The read, write, burst read, burst write and repeated start transmissions are automatically recognized by the core. The core incorporates all features required by the I^2C specification. The DI2CSB supports all transmission speed modes.

LICENSING

Comprehensible and clearly defined licensing methods **without royalty-per-chip fees** make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.

Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core:

- VHDL or Verilog RTL synthesizable HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM Netlist

APPLICATIONS

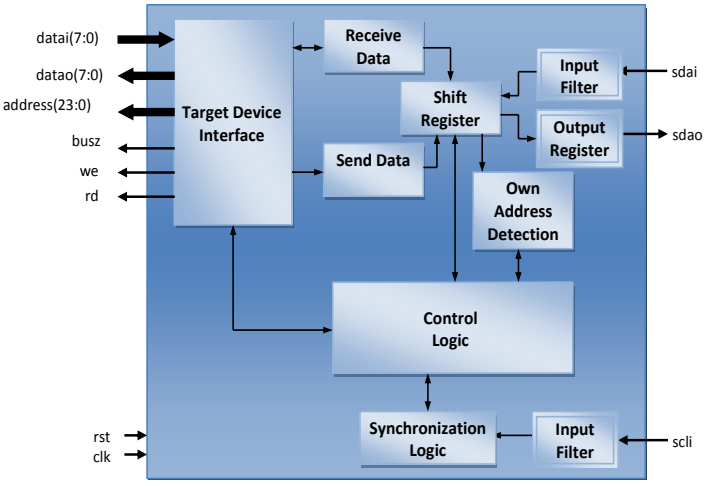
- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Cost-effective reliable automotive systems

KEY FEATURES

- Conforms to v.4.0 of the I^2C specification
- Slave operation
  - *Slave transmitter*
  - *Slave receiver*
- Support for all transmission speeds
  - *Standard (up to 100 kb/s)*
  - *Fast (up to 400 kb/s)*
  - *Fast Plus (up to 1 Mb/s)*
  - *High Speed (up to 3,4 Mb/s)*
- Allows operation from a wide range of input clock frequencies
- Support for reads, writes, burst reads, burst writes, and repeated start
- 7-bit addressing
- No programming required
- Simple interface allows easy connection with target device e.g. memory, LCD display, pressure sensors etc.
- Fully synthesizable
- Static synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan test ready

BLOCK DIAGRAM

The figure below shows the DI2CSB IP Core block diagram.



PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
datai(7:0)	input	Data bus from target device
scli	input	I^2C bus clock line (input)
sdai	input	I^2C bus data line (input)
datao(7:0)	output	Data bus to target device
address(23:0)	output	Address of accessed register
busz	output	Turns datao into Z state
wr	output	Write strobe for target device
rd	output	Read strobe for target device
sdao	output	I^2C bus data line (output)

DI²CX CORES OVERVIEW

The main features of all Digital Core Design I²C compliant cores have been summarized in the table below. It gives a brief member characteristic, helping you to select the most suitable IP Core for your application.

Design	I²C specification version	Master operation	Slave operation	CPU interface	Passive device interface	Interrupt generation	Clock synchronization	Arbitration	7-bit addressing	10-bit addressing	Standard mode	Fast mode	Fast Plus mode	High-speed mode	User defined timing	Spike filtering
DI2CM	3.0	✓	-	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
DI2CS	3.0	-	✓	✓	-	✓	✓	-	✓	-	✓	✓	✓	✓	✓	✓
DI2CSB	3.0	-	✓	-	✓	-	-	-	✓	-	✓	✓	✓	✓	-	✓
DI2CMS	3.0	✓	✓	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

I²C Cores summary table

UNITS SUMMARY

Target device Interface – Performs the interface functions between DI2CSB internal blocks and target device. Allows easy connection of the core with passive devices e.g. memory, LCD display, pressure sensors, I/O devices etc.

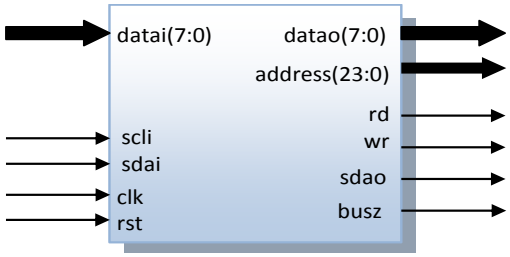
Control Logic – Manages execution of all commands sent via interface. Synchronizes internal data flow.

Shift Register – Controls SDA line, performs data and address shifts, during the data transmission and reception.

Input Filter – Performs spike filtering.

Synchronization Logic – Synchronizes data and address shifts, during the data transmission and reception. SCLI spikes are filtered by this unit.

SYMBOL



DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates, minor and major versions changes
    - Phone & email support

PERFORMANCE

The following table gives a survey about the Core area and performance in INTEL FPGA® devices after Place & Route (all key features included):

Device	Speed grade	Logic Cells	F_{max}
MERCURY	-5	95	220 MHz
STRATIX	-5	95	230 MHz
CYCLONE	-6	95	195 MHz
APEX II	-7	95	220 MHz
APEX20KC	-7	95	170 MHz
APEX20KE	-1	95	130 MHz
APEX20K	-1	95	94 MHz
ACEX1K	-1	95	99 MHz
FLEX10KE	-1	95	95 MHz
MAX 7000AE	-4	50	107 MHz
MAX 3000A	-4	50	107 MHz
MAX II	-3	75	154 MHz

Core performance in INTEL FPGA® devices

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